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Technical Activities Forum

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Engineering of Computer-Based Systems: Current Status and Technical Activities

Stephanie White, *Northrop-Grumman and ECBS TC Chair*
Jerzy Rozenblit, *University of Arizona*
Bonnie Melhart, *Texas Christian University*

Computer-based systems affect virtually everything we do. Typical systems that are computer based include telephone and communications, process control and manufacturing automation, space travel, transportation (automotive, train, aircraft, and air traffic control), command and control, medical instruments, and large or distributed database systems.

Specifically, computer-based systems (CBSs) are those whose behavior is, to a substantial degree, determined or controlled by computers. CBSs tend to be complex, often consisting of many networked, geographically distributed subsystems, and each subsystem may itself be a multicomputer system. A CBS is software, hardware, and frequently communication intensive, and its functional, performance, and reliability requirements mandate tightly integrated information processing and physical behavior.

Interdisciplinary approach

The integration of information technologies dramatically increases the interactions among physical components and processes, generates complex dynamics, and creates component interdependencies unknown in earlier systems. Although development processes for the individual components exist, they remain largely fragmented. Thus, we need a system-level discipline and interdisciplinary engineering specialty—engineering of computer-based systems (ECBS)—that addresses the qualities and challenges of CBSs.

Such interdisciplinary engineering specialties have long existed for other domains—for example, aeronautical, marine, and chemical engineering—but not for CBS. ECBS encompasses many facets: CBS modeling, requirements specification, simulation, architectures, communications, safety, security, reliability engineering, software, hardware, human-computer interfacing, CBS integration, verification and testing, and project management. ECBS takes a holistic approach, addressing these system-development issues and the necessary trade-offs. It aims to integrate systems engineering of CBS with the detailed design and realization of engineering fields such as software, hardware, or codesign into a complete engineering discipline.

ECBS TC formed

The IEEE Computer Society's Technical Committee (TC) on ECBS was officially chartered last November. The mission of our new committee is to

- serve as a forum for the exchange of ideas and for the collection and dissemination of knowledge among inter-

ested practitioners, researchers, and students;
- facilitate and encourage research in the field;
- establish a framework for ECBS professional and academic education and training; and
- promote the ECBS discipline.

The ECBS TC promotes this emerging discipline through technical meetings, workshops, conferences, publications, and activities of the various working groups established as part of our organization. In particular, the International Symposium and Workshop on Systems Engineering of Computer-Based Systems was held in Tucson, Arizona, March 6-9, 1995. Sponsored by IEEE and the University of Arizona, the meeting was attended by researchers and practitioners from 13 countries, representing private industry, government organizations and contractors, and academic institutions. More than 50 refereed papers were presented in parallel sessions organized along major ECBS themes.

Conference themes

Domain analysis and model reusability was a common theme in many presentations. The focus was on developing families of related computer-based results related systems. The papers overviewed existing domain-modeling paradigms and systems, described techniques for developing reusability requirements, and discussed product design with reusable components.

Participants in the systems engineering, design, and analysis track strongly advocated object-oriented techniques for developing ECBS structural, functional, and dynamic models. They presented design techniques and architectures to capture design process models and to support embedded-systems development. Tools and techniques for requirements capture (legacy systems) and specification were discussed. The use of highly structured techniques was demonstrated on a comprehensive example of a groundwater analysis system. Knowledge-based concepts were shown to support intelligent requirements elicitation, and a formal axiomatic approach to specify VLSI requirements was demonstrated.

The contributions to the ECBS process and models track had a distinct systems-theory-inspired flavor, one that advocates a hierarchical, modular approach to design and development. Several papers discussed the formal underpinnings of the ECBS process. Others reported initial, exploratory studies of heterogeneous systems development.

New to our community were the contributions in hard-

ware/software codesign and electronic design automation (EDA). The codesign papers focused on partitioning, system evaluation, and computer-aided support for the design of heterogeneous systems that comprise software and hardware components. The techniques discussed in this session included abstract systems specifications, fuzzy-logic-based design concepts, and the use of concurrent engineering techniques for codesign environments development. The major EDA issues discussed at the meeting were a clustering approach to delay minimization, a cache architecture for a multiview memory model, and a new VHDL-based, interfacing object-oriented language for signal processor developers.

Working group reports

Working group meetings were held during the Tucson conference. Some working groups have held detailed discussions at other meetings over the past few years, while others are in formative stages. Such roundtable discussions have resulted in identification of problems and progress toward solutions. Progress in three areas—process and information modeling, standards, and research—is summarized below.

Process Working Group. The Process WG reviewed and modified draft behavior models of the ECBS process and draft information models for process steps. The group adopted a basic, draft ECBS process model that repeats a single seven-step core process. The core process is applied twice—first to the context and then to define the subject system—at each tier of decomposition. The tiers include domain analysis, concept analysis, system analysis, and subsystem analysis, down to specification of hardware, software, and operator tasks. What changes at each tier is the subject matter to which the core process is applied. At each tier, a rigorous set of requirements and a near-optimal architecture emerge and an implementation plan is produced. (Process WG information contributed by David Oliver.)

Standards Working Group. Although just formed at the Tucson meeting, the Standards WG came to agreement concerning its ECBS charge: to be the ombudsman for the ECBS TC in the standards community, to promote best ECBS practice in related standards, and to employ the model-based approach that is evolving in ECBS as a basis for standardization. The group specifically identified three major action items: (1) work towards describing the new IEEE P1220 standard (Application and Management of the Systems Engineering Process) in terms of the ECBS process and information models, (2) identify existing and planned architecture-related standards that should be taken into account by the Architecture WG, and (3) interact with the Case Study WG in promoting case studies that demonstrate the applicability of the ECBS model-based approach. (Information contributed by Harold Lawson.)

Research Working Group. This WG took on responsibilities to establish the core of ECBS research and clearly discriminate it from work done by systems and software engineering practitioners. The WG's function is to identify research agendas and new paradigms, to act as a

conduit between industry and the ECBS community, and to develop a plan for establishing collaborative, funded ECBS projects. Discussions at this meeting resulted in a list of many ECBS research areas. The list will be refined and used as a guide for encouraging future endeavors by practitioners and researchers.

JOINING THE ECBS TC
We invite your participation in shaping this emerging discipline. As an ECBS TC member, you will enjoy working with an active group of enthusiastic professionals. New know-how will be available to you for use in your daily engineering efforts, and for education and training activities, through formal conference contributions, small group discussions, and newsletters.

Working groups. These groups are an excellent way to participate. Choose one in which you are interested, and contact one of the chairs listed below.
Architecture WG: Hugo Simpson (hugo.simpson@def.bae.co.uk) and Wilhelm Rossak (rossak@pluto.njit.edu)
Case Studies WG: Gerhard Schweizer (mvoss@ira.uka.de)
Information and Process Models WG: Dave Oliver (oliverdw@crd.ge.com) and Ken Jackson (100420.2624@compuserve.com)
Education and Training WG: Jonah Lavi (lavi@math.tau.ac.il) and Bill McCumber (mccumber@lfs.loral.com)
Forensics WG: Darren Dalcher (dalched@vax.sbu.ac.uk)
Reengineering WG: Mark Wilson (mlwilso@relay.nswc.navy.mil) and Gil Meyers (gmyers@code413.nosc.mil)
Research WG: Jerzy Rozenblit (jr@ece.arizona.edu) and Bernhard Thome (bernhard.thome@zfe.siemens.de)
Standards WG: Harold Lawson (bud@damek.kth.se)
Systems Evaluation WG: Perry Alexander (perry.alexander@uc.edu)
Tools WG: Janos Sztipanovits (sztipaj@vuse.vanderbilt.edu)

TC mailing/e-mail lists. If you want to be included in the ECBS TC hard-copy mailing list, contact Elliot Chikofsky (e.chikofsky@computer.org). To add your name to the ECBS e-mail bulletin board, send a message to ecbs-request@riogrande.cs.tcu.edu. There is no fee for TC or working group membership and newsletters.

References. For more information on current ECBS practice and ongoing work, refer to these recent publications:
Lavi, J.Z., et al., "Computer-Based Systems Engineering Workshop," *Proc. SEI 1991 Conf. on Software Engineering Education, Lecture Notes in Computer Science,* No. 536, Springer Verlag, 1991.
Lawson, H., ed., *Proc. 1994 Tutorial and Workshop on Systems Engineering of Computer-Based Systems,* Order No. 5715, IEEE Computer Society Press, Los Alamitos, Calif.
Melhart, B., and J. Rozenblit, *Proc. 1995 IEEE Int'l Symp. and Workshop on Systems Engineering of Computer-Based System,* Order No. 95TH8053, IEEE Service Center, Piscataway, N.J.
White, S., et al., "Systems Engineering of Computer-Based Systems," *Computer,* Nov. 1993, pp. 54-65.
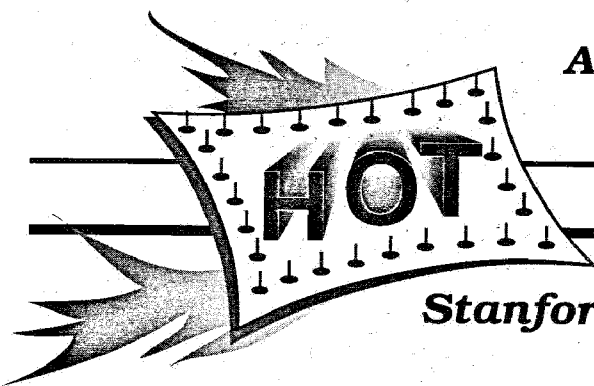
A Symposium on High-Performance Chips

HOT Chips VII

Stanford, California August 13-15, 1995

Stanford University — Memorial Auditorium

Attend HOT Chips VII, a symposium on high-performance chips, which will bring together researchers and developers of chips used to construct high-performance workstations and systems. Enjoy the informal format offering technical interaction with speakers. The first six HOT Chips Symposiums were huge successes and prompted articles in special issues of *IEEE Micro* magazine. HOT Chips VII will again bring you the latest developments in chip technology.

Sunday, August 13 — Tutorials, Luncheon, Wine & Cheese Reception

Morning Tutorial **Custom Parts for Graphics?** by Frank Crow, Interval Research
Afternoon Tutorial **The X86, From Soup to Nuts** by John H. Wharton, Applications Research
4:30 — 6:00 Wine and Cheese Reception for all conference attendees

Monday, August 14

Welcome & Opening Remarks

Embedded Processors
- The First Superscalar 29K Family Member, AMD
- The Elentari Integrated x86 Processor: Architecture and Performance, National Semiconductor
- Superscalar MIPS-II Microprocessor for Core-Based ASIC, LSI Logic

Keynote Speaker
Gordon Moore, Chairman of Intel Corporation

x86 Processors
- The Impact of Dynamic Execution Techniques on the Data Path Design of the P6 Processor, Intel
- The AMD K5 Processor, Advanced Micro Devices
- Building a Better Beast: Native vs. RISC-Like vs. VLIW Implementations of x86 Processors, Cyrix

SPARC Processors
- Performance Evaluation of the Superscalar, Speculative Execution HaL SPARC64 Processor, HaL Computer Systems
- SPARC64+: HaL's Second Generation 64-bit SPARC Processor, HaL Computer Systems
- UltraSPARC-I: A 64-bit Superscalar Processor with Multi-Media Support, Sun Microsystems

Monday Evening Buffet Dinner

Evening Panel Session
Will the x86 Architecture Eat the World?

HOT Chips VII is sponsored by the Technical Committee on Microprocessors and Microcomputers of the IEEE Computer Society. This is an advance program. Presentations may be dropped, added or moved between sessions.

Tuesday, August 15

MPEG
- A Two-Chip Realtime MPEG2 Video Encoder with Wide Range Estimation, NTT
- VLSI Architecture of the I-Frame Encoder for the MPEG-2 Video Compression, IBM
- A Scenic View, S3

Graphics and Compression
- 3D Graphics Processor Chip Set, Fujitsu
- A Single Chip VideoCD with Hi-Fi Audio for Consumer Applications, Integrated Information Technology
- Highly Reliable and Low-CPB IBMLZ1 Compression Algorithm and Technology for Storage Controller, IBM

Parallel and Vector Processing
- Breakthroughs in Parallelizing Compilers and their Architectural Implications, Stanford University
- Scylla: A Memory Controller with Integrated Protocol Engines for Distributed Shared Memory Support, Sun Microsystems
- The T0 Vector Microprocessor, UC Berkeley
- A 150MHz Superscalar RISC Processor with Pseudo Vector Processing Feature, Hitachi Ltd. and University of Tsukuba

RISC
- Balancing Data and Instruction Paths with Execution Engine Requirements in the 64 bit PA-8000, Hewlett Packard
- The First PowerPC PDA Microprocessor, Motorola
- A New Incarnation of the 32-bit PowerPC RISC Microprocessor, Somerset PowerPC Design Center, Motorola and IBM
- The MIPS T5 Microprocessor, Silicon Graphics

Closing Remarks

Check the World Wide Web for Program Updates:
http://dice.scu.edu/HotChips OR http://www.hot.org/hotchips

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Housing Information Requested ☐

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    Date   Time   Date   Time

FEES: Circle appropriate values

	Before July 24th	After July 24th
IEEE/Computer Society or ACM Member	$160	$230
Non-Member	$230	$290
Student Member	$55	$100
Sunday Tutorials, Member	$30	$45
Tutorials, Non-Member	$45	$60
Tutorials, Student	$20	$30
Extra Copy of Notebook (With no mailing)	$30	$30

Registration Includes:

- Attendance
- One copy of the notes
- Two luncheons
- Coffee breaks
- Sunday evening wine and cheese reception
- Monday evening dinner
- Parking

A Stanford map, parking permit, the location of parking, and a receipt will be mailed to early registrants.

On-Site Registration is available on Tutorial Sunday morning and each morning at the Symposium. Early advanced registration is recommended.

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Wire registration, paid via VISA or MasterCard use:
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Use certified mail for registration confirmation.

Questions: Phone: (415) 941-6699
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Registration by mail: Dr. Robert G. Stewart
               Stewart Research Enterprises
               1658 Belvoir Drive
               Los Altos, CA 94024   [c]

Register by July 24, 1995, for lowest rates...