Packaging Design Support Environment -- A Simulation System for Analysis of VLSI Interconnects

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Abstract

An X-Windows based simulation environment has been developed for the prediction of electrical characteristics of integrated circuit packaging structures. This program, called Packaging Design Support Environment (PDSE), applies simulation management techniques to drive several tools that make these calculations. Two tools calculate inductance and capacitance for multiconductor, multidielectric, two-dimensional structures with lossy dielectrics. A third tool uses these parameters to compute pulse response characteristics of multiple coupled, uniform, lossless transmission lines terminated at discrete points with "R", "L", and "C" elements. The design process in PDSE proceeds in three major phases: modeling, simulation, and evaluation. These processes are interactive and allow the designer to refine a design model, modify experiments, and apply various evaluation procedures.

1. Introduction

Advances in semiconductor technology have brought about a dramatic increase in speed of operation of silicon devices and integrated circuits. As signal rise times become shorter than 1 ns, the electrical performance of interconnections becomes an important factor in the design process. The behavior of interconnections has become an important issue in VLSI packaging because of the "crosstalk" and reflections which increase as the density of packaging becomes higher [1].

Performance estimation in these systems involves the analysis of transients caused by pulsed voltages. The transient behavior of interconnections is modeled by the transmission line equations

$$\partial v / \partial z = -Ri - L\,\partial i / \partial t$$

$$\partial i / \partial z = -Gv - C\,\partial v / \partial t$$

where $v = v(z, t)$ and $i = (z, t)$ are the n-dimensional vectors of line voltages and currents and $z \in \{0, l\}$, with l being the line length. The symbols "R", "L", "G", "C" represent the matrices of resistances, inductances, conductances, and capacitances, respectively. The entries of these matrices are computed from the engineering specifications of interconnections [2]. Because of the complex nature of predicting the electrical performance (crosstalk, delay, pulse distortion, etc.) of interconnections, computer simulation tools have been developed which use the relationships above to estimate the performance of interconnect systems. Details describing these calculations are available in [2], [3], and [4].

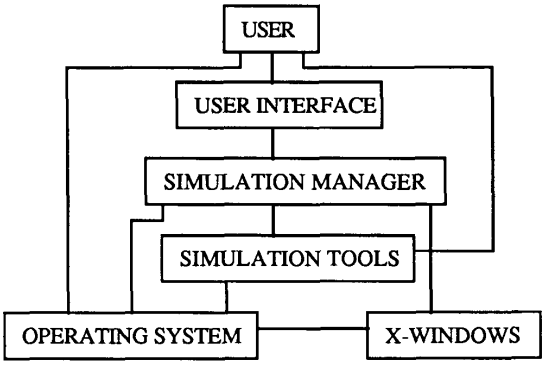

Figure 1. PDSE block diagram.

This paper describes a software environment, Packaging Design Support Environment (PDSE), which was developed to assist the VLSI package engineer in efficiently evaluating the integrity of interconnect systems. It accomplishes this by combining the user-friendliness of a menu-driven graphics system with the power and speed of the interconnect analysis tools mentioned above. Figure 1 shows a block diagram of PDSE's architecture. The user may directly use any of the simulation tools or operating system utilities, or may access the tools and operating system through the graphical user interface. The simulation manager uses experimental frames (a set of circumstances under which a given model is observed [5]) to assist the user in specifying variations

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of a model to be tested (ie. a description of an interconnect system) and specifying varying sets of data with which the model is to be tested.

2. VLSI Packaging Simulation Tools

A typical interconnection system can be decomposed into terminating networks, sections of multi-conductor parallel lines, and discontinuities (bends, junctions, cross-overs, vias, etc.) [6]. The terminating networks are modeled utilizing lumped parameter equivalent circuits for the components like transistors, independent sources, and R, L, C elements. The mathematical models of networks are determined using well established circuit analysis techniques. The sections of multi-conductor parallel interconnections are modeled as multi-wire transmission lines described by one-dimensional wave equations. The discontinuities are replaced by their lumped parameter equivalent circuits [1]. Several tools have been developed to simulate the transients on such interconnect systems.

Coupled Line Simulator (UACSL) [7] is a tool that simulates the transient response of a general linear network containing resistors, conductors, capacitors, inductors, coupled inductors, piecewise linear independent voltage sources, and lossless uniform transmission line systems. Up to 50 independent voltage sources, 10 transmission line systems, and 100 of each type of component may be specified. Each transmission line system can be composed of up to ten conductors and must be described by their length and by the capacitance and inductance matrices as calculated by one of the parameter calculators described below.

Method of Moments TEM transmission Line Parameter Calculator (UAMOM) [8] and UA Capacitor Calculator (UAC) [9] calculates the capacitance and inductance matrices (per unit length) of a parallel multiconductor transmission line system given its cross-sectional geometry. Lines are assumed to be of infinite length, and end effects are not calculated. Ground planes and dielectric interfaces are taken as infinite in extent. Up to ten conductors may be specified, and each conductor may have up to twelve sides. The specific limitations of each tool are described below.

UAMOM allows up to six dielectric layers to be specified. The moment calculator evaluates the TEM line parameters for geometries that lie in one of the categories below:

1. One infinite ground plane present, finite ground conductors allowed.
2. Two infinite ground planes present, finite sized conductors allowed.
3. Only finite sized ground conductors present.

Up to ten arbitrarily shaped conductors may be defined, any number of which may be designated as ground conductors. Conductors may intersect with any number of dielectric interfaces, but must not touch each other or ground planes.

The allowable geometries for UAC are more limited than those allowed for UAMOM, but the results tend to converge more consistently for UAC than for UAMOM [6]. These geometries are described below:

1. One finite ground conductor, no ground planes, two dielectric layers.
2. One infinite ground plane, no finite ground conductors, two dielectric layers.
3. Two infinite ground planes, no finite ground conductors, one dielectric layer.

In each case every conductor must lie wholly within one dielectric medium. conductor placement is arbitrary as long as the conductor does not touch any ground plane, dielectric interface, or other conductor.

3. PDSE Simulation Manager

Experimental frames are used to simulate several variations of a model with several variations of input to the model. There are three steps in performing a coupled line analysis in PDSE -- create the model(s), define the experimental frame(s), and run the simulation(s).

PDSE allows the user to define (or retrieve from a model data base) up to ten variations of any given model [10]. For example, it may be desired to analyze an interconnect system given different termination networks. Through menus, the user would specify the resistors, capacitors, inductors, coupled inductors, voltage sources, and transmission line systems that make up the given system. PDSE prompts the user to specify the number of variations of this model that are to be created. It then guides the user in the creation of each of these models.

The experimental frame is defined independently of the models. It consists of a set of input waveforms for each voltage source and a set of control variables (which allow the user to monitor the simulation). Up to ten waveforms may be defined. The waveforms may be defined as a set of step inputs with a range of up to ten different rise times, or may be a set of up to ten generic waveforms defined by piecewise linear segments. The user may define a set of maximum allowable voltages for each probe point in the circuit. This allows the user to monitor each probe point to know if an unacceptable voltage ever appears on that node.

Once a set of models and an experimental frame have been defined, the simulation process may begin. Management of the simulation process is illustrated in Figure 2.

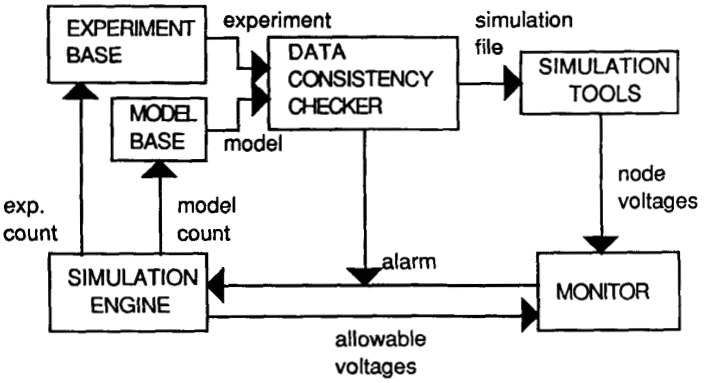

Figure 2. Simulation Manager block diagram.

The Simulation Engine controls the simulation process. It informs the model base which interconnect specification to use, and transmits the appropriate waveform to the Data Consistency Checker. The Data Consistency Checker has been designed so that inconsistent or missing data will be automatically replaced when possible. When this is not possible, the user is informed about the problem, and the simulation process is not started until the discrepancy is corrected. The Monitor watches the node voltages of each probe point and sends an alarm to the Simulation Engine whenever a voltage greater than the maximum allowable voltage appears on any probe point

When UACSL is to be executed, the Data Consistency Checker verifies that there are capacitance and inductance matrices provided for each transmission line system. If they have not been provided, UAMOM or UAC will automatically be executed to calculate these values. The user is informed of this process, but no user intervention is required.

4. Post Processing/Data Analysis

One of the most important parts of any simulation is the analysis and application of the simulation results. PDSE was designed to help the user quickly understand the results of package simulations and apply those results to improve the package design. Currently, there are two sets of results available once a set of simulations is complete. A graphics display window is provided to display the probe voltages calculated for each probe point of each circuit. These plots are of the voltage levels vs. time at the circuit probe points specified by the user. The second type of results which are available is a compilation of all the probe points on which voltages appeared that exceeded the maximum allowable level for that specific node.

These features aid the designer in evaluating various package models. Other questions that may be answered by the appropriate analysis of the data are, "What is the settling time on line x?," "Do the voltages on line x monotonically cross some window threshold?," and "What is the voltage steady-state error on line x?." Although PDSE does not yet automatically answer these questions, it is planned to add knowledge-based evaluation procedures which will answer these and similar questions. Given this capability, PDSE would then be used to rank the models based on various design criteria (ie. speed, chip size, cost, etc.) Not only will PDSE rank design models, but it will offer suggestions on how to improve designs. The models could then be modified, re-simulated, and re-evaluated.

5. User Interface

The main purpose for designing PDSE was to provide the user with a robust, user-friendly environment which integrates the simulation tools mentioned above. This was accomplished not only by implementing experimental frames but by designing a modular easy-to-use, easy-to-learn graphical interface. This graphical interface includes pop-up menus, dialogue boxes, spread-sheet like windows, and plotting windows and is based on the X-Windows graphics package.

6. Summary

PDSE provides a user-friendly environment for modeling and simulating the electrical characteristics in VLSI packages. The experimental frame facilitates the evaluation of various package design models. Users are able to efficiently simulate several variations of an interconnect package design based on varying inputs. The results of these simulations are graphically displayed. This allows the user to easily make design choices based on the simulation results.

PDSE will eventually be integrated with computer automated design tools. This will enable it to directly read interconnect layout information from the CAD tool layout description files, analyze the input from the netlist, and guide the user to improved design choices.

Acknowledgement

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