INTELLIGENT DESIGN AUTOMATION OF VLSI INTERCONNECTS

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ABSTRACT

Interconnection and packaging are among the dominant factors that limit the performance of future integrated circuits containing millions of transistors. As chips become more complex, so does the packaging. Design automation is thus without doubt necessary. In this paper, a window based simulation environment called PDSE (Packaging Design Support Environment) which integrates several tools for VLSI interconnection modeling and simulations is presented. We will describe the concept of the automated packaging design cycle, the structure and the components of the simulation environment, and the implementation of an interconnect layout geometry data extractor. Finally a case study will be given to illustrate the entire design process.

Introduction

The study of VLSI interconnections has become an important issue in packaging because the undesired phenomena such as crosstalk and reflection increase as the density of packaging and signal propagation speed increase. Although this is true, the development of models and simulation tools for design of electronic packaging structures still lags the development of tools for chip design in many respects, especially in the electrical performance area [1]. The ability to analyze and verify the packaging designs including the circuit consideration, geometry, and material etc. is as necessary for packaging structures as for chip designs. Our approach for analyzing the electrical performance is primarily based on the study of the transient behavior of the interconnections modeled by transmission lines system. Because of the complex characteristics of the interconnections, computer simulation tools are applied. So far, two major groups of computer tools for the analysis and design of VLSI interconnection have been developed at the University of Arizona. The first group is composed of parameters extraction tools which calculate the capacitance matrices, inductance matrices and resistance matrices for the multiconductor, multidielectric, two–dimentional structures . The tools in the second group are coupled transmission lines simulators for the estimation of electrical characteristics such as crosstalk, delay, pulse distortion, etc. The simulations are based on the uniform and lossless transimission lines model. In addition to the two major groups of tools, there is a CAD data base extractor which can extract the cross sectional geometry of the conductors directly from the layout interconnect description. The extracted data, after format conversion, can be processed by the group one tools for parameter extractions. All the softwares described above are well organized and easily accessed by an X window based support environment called PDSE (Packaging Design Support Environment) [2]. With easy–to–access graphical interface like pop–up menus, dialog boxes, spread–sheet windows, and plotting windows, the augmentation of the whole system is still under way in order to automate the entire design phases. The automated design cycle we are developing here can be illustrated in Figure 1. Basically, the VLSI packaging design is a process of incremental refinement(redesign) driven by the interactions among the model base, simulation tools and performance evaluation according to the specifications and design goal. For parameter extraction tools, the user has to define the coupled transmission lines model. This includes specifying a set of parallel multiconductors' cross sectional geometry and the dielectric constants. Up to ten conductors may be specified in PDSE now, and each conductor may have up to twelve sides. For the transmission lines circuit simulators, the user has to construct the models of transmission line system (includes coupled transmission lines and terminating networks) and the input waveform. The per unit length L, C matrices of the coupled transmission lines are the results calculated from parameters extraction tools. The user can also specify

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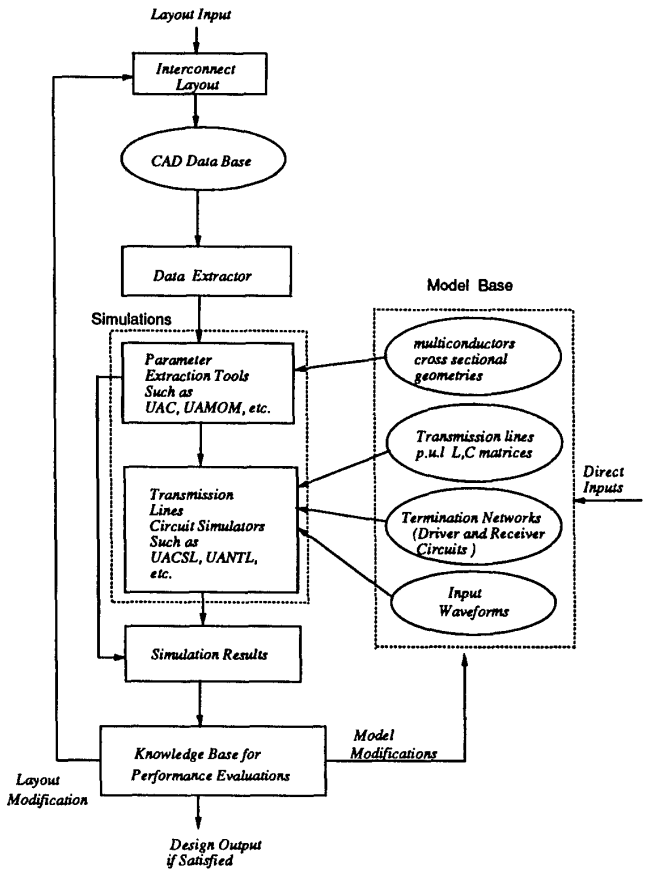

Figure 1: The flow chart of packaging design automation.

the matrices directly instead of supplying the information of the cross sectional geometry. For the termination networks such as drivers and receivers, the parameters of the lumped model's components such as transistors, independent sources, resistance, conductance, and inductances must be specified. PDSE allows the user to define up to ten variations of any given model so that it can analyze an interconnection system given different termination networks [3].

The models of the waveforms are served as the inputs to the voltage source in the termination network. Up to ten waveforms may be defined. The waveforms may be defined as a set of step inputs with a range of up to ten different rise times, or may be a set of up to ten general waveforms specified by piecewise linear segments. The data extractor can extract the cross section geometry of the multiconductors directly from the interconnect layout drawings from the CAD graphic tools. The information can then be processed by the parameter extraction tools via data format conversion. After simulation, the results will be evaluated by the design knowledge base. Rule based reasoning will be carried out according to the design constraints and design goal. Thereafter, suggestions for modifying related parameters in the model base or the geometry in the CAD graphic tools will be given for the purpose of redesign until the final results satisfy the design specifications. The following sections describe the theoretical foundations and implementations for the components of the PDSE architecture.

Data Extractor

The data extractor is designed as the preprocessor for parameter extraction tools. Our idea is to extract the interconnect description from a universal file format so that any CAD tool that conforms to such file format may be interfaced with PDSE. This can minimize the labor of human interaction in inputting the cross section geometries of multiconductors. We have focused our effort on the support of DXF (Drawing eXchange Format) file import. There are several reasons for this: 1) The majority of the industrial companies use Autodesk's AutoCAD for their layout graphics. 2) Autodesk's DXF format is used for CAD data interchange in addition to IGES. 3) DXF file is suitable for three dimension expansion. 4) AutoCAD is capable of supporting DXF import and export. 5) DXF file is an ASCII file. It is easier to process the ASCII file than the binary drawing file. The extraction procedures in our system now include: 1) define the extraction region on the AutoCAD drawing file. 2) export the DXF format of the extraction region from AutoCAD. 3) AutoCAD is an object–oriented CAD tool. In this step, we use our routine to identify and calculate the cross section geometries of the objects(conductors) in the DXF file. 4) interfacing the different data formats between PDSE and the derived geometry information in 3). The data extractor now handles two dimensional layout drawings. The user has to specify the thickness of the conductor from their design information.

Parameter Extraction Tools

Parameter extraction tools are used to determine the per unit length (p.u.l) inductor (L) matrix and capacitance (C) matrix for a multiconductors transmission line system. The L,C matrices are computed based on the conductors cross sectional geometry and substrate permittivity. Once the L, C matrices are obtained, then they are passed on to the circuit simulators for transient analysis. There are two parameter extraction programs in PDSE, one is called UAC and the other is called UAMOM. UAC [2] calculates the p.u.l. L,C matrices by assuming quasi–static fields for parallel multiconductor systems. The lines are assumed to be of infinite length and end effects are not included. UAC provides good numerical convergence at an expense of large CPU time. UAMOM [4] also computes the p.u.l. L,C matrices for parallel multiconductor systems; it is based on the method of moments and TEM assumption. UAMOM provides greater flexibility in terms of the number of dielectric substrates and conductors cross sectional geometry. UAMOM only requires moderate memory storage and CPU time.

Circuit Simulators

Circuit simulators are used for calculating the transient responses of electrical networks. There are two circuit simulators in PDSE. (1) UACSL [5] computes the transient response of multiconductor interconnections with linear terminal networks (i.e., only with lump resistor, capacitor and inductor elements). (2) UANTL [6] performs the same analysis as UACSL but allowing nonlinear terminal networks (i.e., diodes, bipolar transistors and MOS transistors). Thus , UANTL requires greater memory storage and larger CPU time (due to large overhead) in comparison to UACSL. The input and output formats of UACSL and UANTL are similar to those of SPICE program in which users specify the circuit element between a pair of nodes. The transient response at any given nodes can be observed through the output windows of PDSE. The transmission line systems in both UACSL and UANTL are composed of multiple lossless conductors, which are coupled together, and can be characterized by their circuit theory parameters, i.e., capacitance matrices and inductance matrices. These matrices are computed by using the parameter extraction tools (UAC or UAMOM) as mentioned in the previous section. The comparisons of our tools to the other similar tools can be found in the referenced papers.

Model Base

Currently, the users of the PDSE have to create the simulation models through a series of menus to specify the resistors, capacitors, coupled inductors, voltage sources and transimission lines geometries for the model base. In order to expedite the design and simulation cycle, realize the rapid prototyping paradigm, the object–oriented programming technique and data reuse concept are introduced. We are developing an object based "macro" library which contains a variety of macro structures for driver networks, receiver networks, transmission lines, and waveforms. Putting all the four kinds of macros together, the user can start simulating the behaviors of the transmission lines system. Every time the user needs a driving network, for example, he does not have to start from the data entry menu to specify the driving network. All he has to do is call the needed driver macro (such as 3μm technology driving circuit macro, etc.) and specify the input/output connection nodes. There is no need to worry about inside details of the driving circuit macro. We can have user built–in (customized) macros and industrial standard macros in the library. An icon based environment is going to support the "macros" library to create our model base.

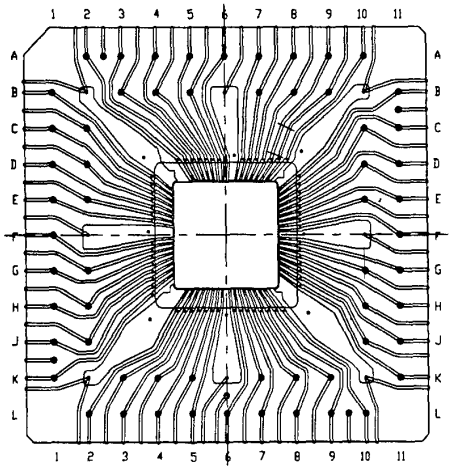

Figure 2: A typical PGA layout with two cut lines defined extraction region on the upper right.

Case Study

A typical 68 lead PGA package layout is shown in Figure 2. The two cut lines are also drawn to define the extraction region (The part for analysis is between the two cut lines).

The DXF file of the extraction region is then processed by the data extractor to get the cross sectional geometry and the average length of the multiconductors. The extracted conductor width is 4.9 mils, the spacing between the two conductors is 8.0 mils and the conductor length 46.7 mils. The results will be directly processed by parameter extraction tools. The conductor cross section geometry is shown in Figure 3.

Noted that the substrate relative permittivity, the conductor's thickness and the substrate thickness cannot be obtained directly from the layout, thus they must be input separately. In order to demonstrate the ability of PDSE, a simple example is used as shown in Figure 4.

Two conductors transmission line system with CMOS drivers (which are nonlinear elements) and each line is terminated by a 0.1 pF capacitor and 82.7 ohms resistor (which is equal to the line characteristic impedance for line matching purpose). The driver of the active line is driven by a fast switching pulse with a rise time and fall time of 30 ps and a magnitude of 5 volt. PDSE first computes the per unit length L,C matrices of the transmission lines system based on the cross sectional geometry and then automatically feeds the information to its circuit simulator. The results of the transient response for various probe points are shown in Figure 5 and Figure 6. Probe 1 represents the input pulse signal. Probe 2 and 3 represent the near end (close to the driver) and far end (close to the load) voltage of the active line (the switching line), respectively. Noticing that there is a time different between the waveform of probe 2 and 3, which is due to the propagation delay of the transmission line. Probe 4 and 5 are the near end and far end crosstalk voltages on the quiet line (nonswitching line), accordingly, as a result of pulse switching on the active line. These crosstalk voltage could cause false switching in digital circuits. In addition, if the transmission line is not terminated properly, additional propagation delay time and false switching of digital circuits may be resulted. The solutions to these undesired phenomena will be addressed in the next section.

Knowledge Base for Performance Evaluation

The simulation results of our first time design may not satisfy our design specifications. For example, the transient response of our case study may greater than the set noise margin. The discrepancy will trigger the knowledge base for the suggestions to improve the performance in order to eventually satisfy our design goals. Three major experts will be integrated into the knowledge base. They are noise expert, wiring expert and delay expert. For example, in order to reduce the crosstalk noise, rule based reasoning will be carried out by the noise expert. The expert may suggest the user to increase the spacing between conductors, to reduce the dielectric permittivity or to reduce the switching speed, etc. On the other hand, to reduce delay, the delay expert may suggest shortening the line length or using the faster signal and the like. Of course, we may not have the luxury to modify every possible parameter. Thus, trade–off must be made. Once we know which parameter can be modified, then the design knowledge base system will provide the exact value of the parameter such that the design goal can be met. For example, to reduce the crosstalk, one of the options is to increase the spacing between conductors. The question is by how much of the conductor spacing is required because we want to keep the conductors as near as we can. One of the efforts that the noise expert will make for finding the optimal spacing is as follows. At first, the original spacing will be doubled and the simulation process

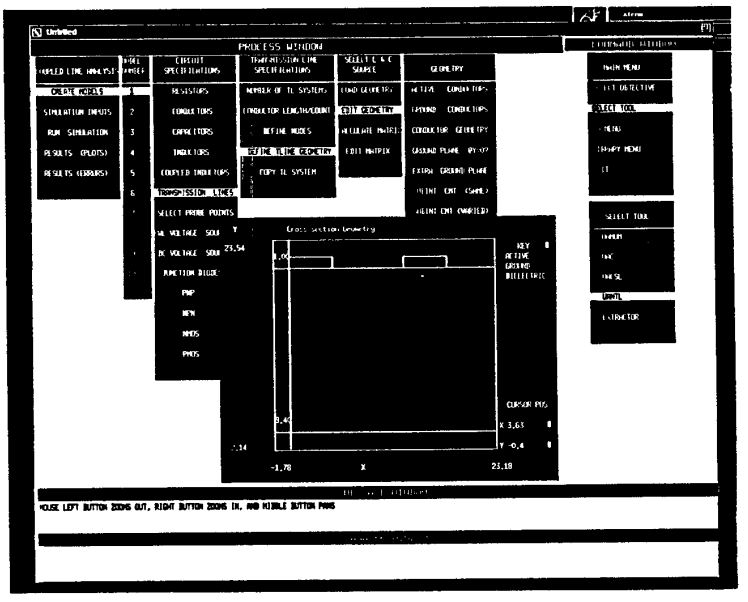

Figure 3: The cross sectional geometry of the extracted layout.

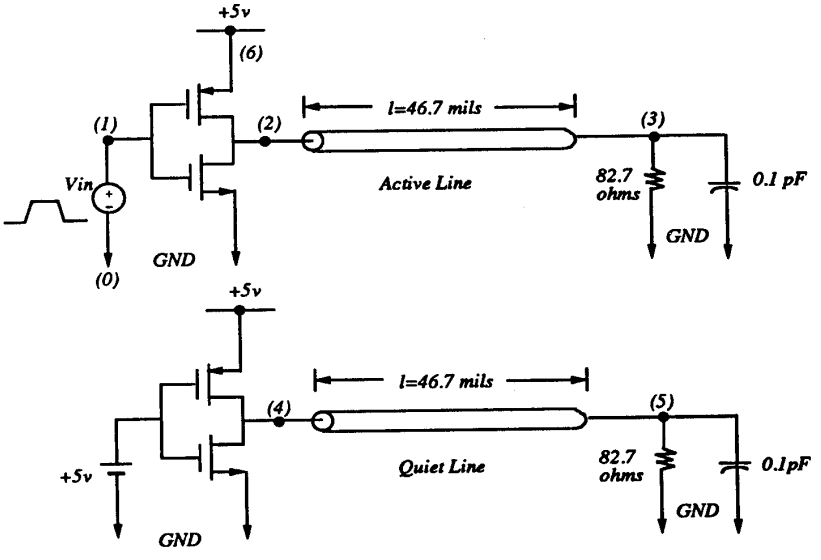

Figure 4: The transmission line system with CMOS drivers and match termination at the load ends.

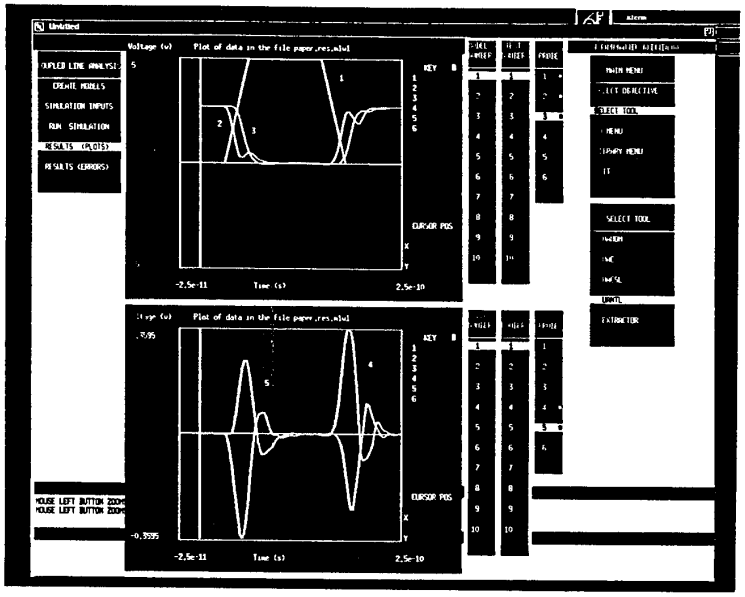

Figure 5: The input waveform and transient response of the circuit diagram in Fig.4.

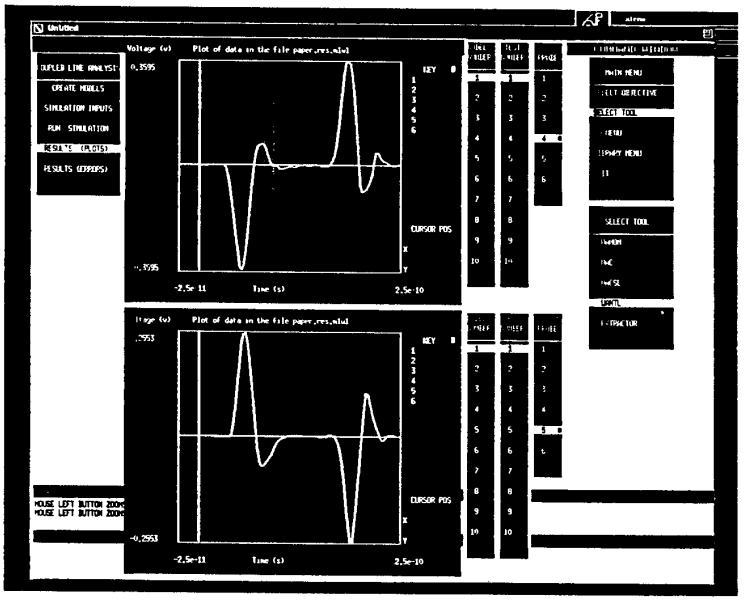

Figure 6: The far end and near end crosstalk voltages on the quiet line.

will be repeated. This means the new spacing information will be processed by the parameter extraction tools to calculate the p.u.l L, C matrices for the circuit simulator. If the output transient response of the circuit simulator meets our design specification, then we know the optimal spacing is between the original spacing and the one we just simulated. We can then apply binary search technique to find the appropriate spacing. Otherwise, we double the spacing until we find the conductor spacing that meets our design constraints. The process is repeated until the optimal spacing is obtained.

Conclusion and Future Directions

This paper describes the whole picture of the design automation for VLSI packaging and interconnections in the electrical performance area. The user interface of PDSE is user friendly, and the usefulness of the simulation environment is briefly illustrated in our case study. We are still augmenting the PDSE so that it will facilitate more design purposes. Several researches are still under way. The two dimensional data extarctor is now expanded to three dimensional one. Eventually the three dimensional layout interconnect information from the CAD graphic tool on the workstation will be extracted directly by our improved data extractor. The application of the knowledge base for the performance evaluation and redesign are developed in two directions. The first direction is to improve the cross sectional geometry of the multiconductors. The other one tries to improve the termination networks. We are now creating the "macro" library. The driver circuit module in our case study is a typical example of the proposed macros. New simulation tools are also continuously added into the PDSE such as UA2DL which calculates the frequency–dependent, per unit length inductance and resistance matrices for multiple, coupled lossy transmission lines.

Acknowledgement

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