Towards a VLSI Packaging Design Support Environment (PDSE); Concepts and Implementation

J.W. Rozenblit, J.L. Prince, and O.A. Palusinski
Department of Electrical and Computer Engineering
University of Arizona
Tucson, AZ 85721
U.S.A

Abstract

A software shell is being developed for assisting in VLSI package design. Called Packaging Design Support Environment, the shell integrates tools for modeling and simulation of electrical characteristics of VLSI packages. Parameter extractors tools calculate inductance and capacitance for multiconductor, multi-dielectric, two-dimensional structures with lossy dielectrics. The simulation tools compute pulse response characteristics of uniform, multiple, coupled and lossless transmission lines. The PDSE shell provides facilities for supporting the package design cycle. Such support facilities include an interface to couple PDSE with a CAD design data base, model and simulation experiment libraries, simulation management procedures that guide evaluation of alternative design models, and data analysis support tools. Expert Systems techniques are being incorporated in PDSE.

1. Introduction

The development of models and simulation tools for design of electronic packaging structures has lagged the development of tools for chip design. Trends in chip and system characteristics and the current state of the packaging art indicate that the ability to verify packaging designs and optimize materials and geometries before hardware is available, is as necessary for packaging structures as it is for chips. The behavior of interconnections has become a crucial issue in VLSI packaging. There are many electromagnetical phenomena that may significantly impact the signal integrity and overall system performance. The problem of predicting interconnections' performance is complex and the use of simulation modeling techniques is necessary prior to the actual design implementation. The simulation of transients in the interconnections is a principal method for acquiring data about the anticipated performance of the system to be designed. Experimentation with hardware prototypes would be prohibitive in terms of expended time, materials, manpower, etc. Thus it is crucial that sophisticated computer-aided tools be available to support design of VLSI packages [1,2].

Over the last several years, we have been developing such tools in the Electronic Packaging Laboratory at the University of Arizona. The programs comprise parameter extractors that calculate inductance and capacitance for multiconductor, multi-dielectric, two-dimensional structures with lossy dielectrics and simulation tools that compute pulse response characteristics of uniform, multiple, coupled and lossless transmission lines. The programs have been integrated into a workstation-based system called Packaging Design System Environment. Our long term objective is to evolve the environment into a package compiler. The compiler would be based on a modeling simulation system for performance, manufacturability, cost, and reliability evaluation of real packaging structures. PDSE is a precursor of such a system. Our strategy is to integrate database and analysis tools, to implement expertise in the form of design rules to address multichip packaging structures, and to interface the workstation environment with physical and electrical design data bases.

At the present time, PDSE consists of the following tools: Method of Moments Transmission Line Parameter Calculator (UAMOM), Capacitance Calculator (UAC), Coupled Line Simulator with Linear Terminations (UACSL), and Coupled Line Simulator with Non-Linear Terminations (UANTL). The modeling and simulation procedures assume the validity of TEM-wave approximation. Thus Maxwell's equations are reduced to Poisson's (or Laplace's) equation in the low frequency limit. The parameter extractors provide capabilities for modeling of inductance and capacitance for multiconductor, multidielectric, two-dimensional structures with lossy dielectrics. The line simulator accepts the L and C matrices and computes pulse response characteristic of uniform multiple, coupled, lossless transmission lines, terminated or loaded at discrete points with R, L, and C elements.

The shell also provides facilities for supporting the package design cycle. Such support facilities include an interface to couple PDSE with a CAD design data base, model and simulation experiment libraries, simulation management procedures that guide evaluation of alternative design models, and data analysis support tools. Currently, Expert Systems techniques are being incorporated in PDSE. The system has several design levels. The lowest level is comprised of the simulation tools. Facilities for model and experiment specification (i.e., experimental frames which

define sets of conditions for running and controlling simulations and processing their results) allow the designers to specify alternative design models and simulation experiments. The separation of models from experiments facilitates flexibility in organizing simulations and in evaluating various design models. More specifically, several alternative models of a package can be evaluated within the same experimental frame and the resulting performance measures can be used to select the best alternative. The simulation management level provides facilities for selection of models, experiments, initialization of simulation runs, and interrupt handling. The next level will include expertise for analysis of simulation data, validation of results, and selection of best designs. The user interface is window and mouse driven. It has flexible graphic tools for representation of conductor geometries and output data.

The design process in PDSE proceeds in three major phases: modelling, simulation, and evaluation. These processes are interactive, allowing the designer to refine a design model, modify simulation experiments, and apply various evaluation procedures. The conceptual framework in which PDSE is grounded is termed Model Based System Design [3,4]. We proceed to briefly describe the principles of this design approach. We then specify PDSE's architecture and its functions in more detail.

2. Model-based System Design

Our methodology for supporting VLSI package design is derived from the model-based system design framework proposed by Rozenblit [3,4]. In this framework, a designer employs modeling and simulation techniques to build and evaluate models of the system being designed. As opposed to system analysis where models are derived from existing real systems, in design the model comes first as a set of "blueprints" from which the system may be built. The blueprints may take several forms; they could be: informal descriptions of the system components, their functions and component coupling specifications, a set of equations, or a computer program representing both declarative and procedural knowledge about the system to be deployed.

The model-based design methodology treats the design process as a series of activities that include: specification of design levels in a hierarchical manner (decomposition), classification of system components into different variants (specialization), selection of components from specializations and decompositions, development of design models, experimentation and evaluation via simulation. Alternative design models are evaluated with respect to *experimental frames* [5], i.e., sets of conditions under which a design model is simulated, that reflect design performance questions. Results are compared and traded off in the presence of conflicting criteria. This results in a ranking of design models and supports choices of alternatives best satisfying the set of design objectives and, subsequently, the choice of a design solution.

The design model development process is driven by the set of objectives, requirements and constraints. Models can be stored in the model base. Thus, in many design situations previously developed design expertise (stored in the form of design models) can be retrieved and used to support the development of a new model.

Performance of design models is evaluated by simulation. A simulation experiment is defined using the experimental frame concept. Briefly, an experimental frame defines a set of input, control, output, and summary variables, and input and control trajectories. These objects specify conditions under which a model can be observed and experimented with. It is usually realized as a coupling of three components: a generator (supplying a model with an input segment reflecting the effects of the external environment upon a model), an acceptor (a device monitoring a simulation run), and a transducer (collecting and processing model output data). We shall return to this concept in Section 3.2.

The simulation phase of our design framework is followed by evaluation of simulation results and ranking of alternative design models in respective experimental frames. Design models that best conform to design performance criteria serve a basis for the proposed design solution.

PDSE is suited for carrying out design within the above framework. We now proceed to describe its architecture in more detail.

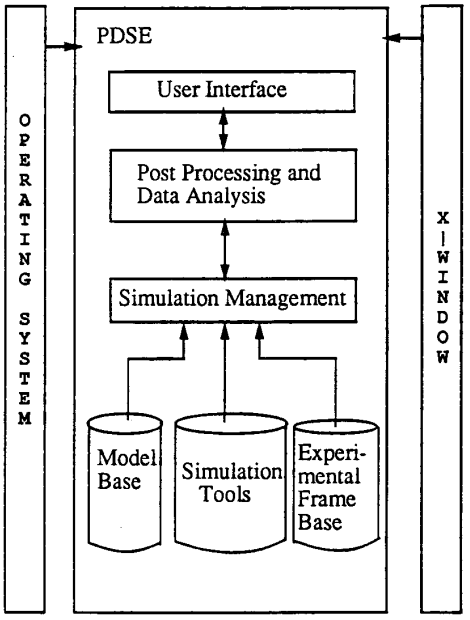

Fig. 1 Architecture of PDSE

3. PDSE: The Architecture and Its Functions

Figure 1 depicts the software architecture of PDSE. The shell is implemented on a DEC VAXstation II/GPX under the Ultrix-32 operating system and the X-windows package.

The levels of PDSE's design are: the electrical simulation modeling tools, model and experiment specification data bases, simulation management procedures, data analysis and post processing modules, and the user interface.

3.1 Parameter Extractors and Simulation Tools

We briefly describe the parameter extractor and simulation tools embedded in PDSE. All programs can be used either as stand alone tools or as modules in a comprehensive analysis of a given design problem. We refer the reader to [6,7,8,9,10] for a detailed description of each program.

The parameter extractors are: Method of Moments TEM Transmission Line Parameter Calculator (UAMOM) [8] and UA Capacitor Calculator (UAC) [9]. They calculate the capacitance and inductance matrices (per unit length) of a parallel multiconductor transmission line system given its cross-sectional geometry. Lines are assumed to be of infinite length, and end effects are not calculated. Ground planes and dielectric interfaces are taken as infinite in extent. Up to ten conductors may be specified, and each conductor may have up to twelve sides. For UAMOM, up to six dielectric layers may be specified. The moment calculator will evaluate the TEM line parameters for geometries that lie in one of the categories below: 1) one infinite ground plane present (microstrip-like), 2) two infinite ground planes present (stripline-like), and 3) only finite sized ground conductors present.

Up to ten arbitrarily shaped conductors may be defined, any number of which may be designated as ground conductors. Conductors may intersect with any number of dielectric interfaces, but must not touch each other or ground planes. To facilitate the calculation of the parameters, all of the conductor sides and dielectric interfaces are approximated by straight line segments (subintervals). The more subintervals per side, the longer the calculation will take. The dielectric interfaces and ground planes must be truncated at a fixed distance from the conductors.

The allowable geometries for UAC are more limited than those allowed for UAMOM. They are: 1) one finite ground conductor, no ground planes, two dielectric layers, 2) one infinite ground plane, no finite conductors, two dielectric layers, and 3) two infinite ground planes, no finite conductors, one dielectric layer.

In each case every conductor must lie wholly within one dielectric medium. Conductor placement is arbitrary as long as the conductor does not touch any ground plane or dielectric interface. As in UAMOM, the number of subintervals per side may be specified for the calculation.

A typical interconnection system can be decomposed into terminating networks, sections of multi-conductor parallel lines, and discontinuities (bends, junctions, cross-overs, vias). The terminating networks are modelled utilizing lumped parameter equivalent circuits for the components like transistors, independent sources, and R, L, C elements. The mathematical models of networks are determined using well established circuit analysis techniques. The sections of multi-conductor parallel interconnections are modelled as multi-wire transmission lines described by one-dimensional wave equations The discontinuities are replaced by their lumped parameter equivalent circuits [6]. Several tools have been developed to simulate the transients on such interconnect systems.

Coupled Line Simulator (UACSL) simulates the transient response of a general linear network containing resistors, conductors, capacitors, inductors, coupled inductors, piecewise linear independent voltage sources, and lossless uniform transmission line systems. Each transmission line system can be composed of up to ten conductors and must be described by their length and by the capacitance and inductance matrices as calculated by one of the parameter calculators described above.

Coupled Line Simulator with Non-Linear Terminations (UANTL) is a program that simulates the transient responses of networks containing resistors, capacitors, inductors, coupled inductors, piecewise linear independent voltage sources junction diodes, bipolar junction transistors (BJT's), MOS transistors (MOSFET's), and systems of lossless transmission lines. The transmission line systems can be composed of multiple conductors which are coupled. There is no coupling between the systems. It is assumed that the transmission lines are fully characterized by their circuit-theory parameters, i.e., capacitance and inductance matrices. These parameters are determined by the geometry and material properties of the interconnections. They are computed by UAC or UAMOM.

3.2 Simulation Management Process

As we have mentioned in Section 1, the separation of models and experiments is the basis for managing simulation studies in PDSE. The model and experimental frame bases facilitate storage and retrieval of alternative models and simulation experiments, respectively. The parameter extractor tools use two dimensional representation of conductors' geometries as described in Section 3.1. To use the simulation tools, we model a network by defining circuit specifications. Resistors, capacitors, inductors, coupled inductors, voltage sources, and transmission line systems are specified using convenient, interactive menus. Each of the components is defined by its connecting node numbers and component values (resistance, capacitance, etc.). To specify a transmission line system, we enter the connection node numbers, transmission line length, and its cross-sectional geometry.

The experimental frame specification consists of:

- An input waveform for each voltage source defined in the model (up to ten waveforms may be defined as a set of step inputs with a range of up to ten different rise times). The waveforms may also be defined by piecewise linear segments.
- The control variables which allow the user to monitor simulation. There are two sets of control variables. First is the simulation length. The second is a set of maximum allowable voltages for each probe point in the circuit. This allows the user to monitor each probe point to know if an unacceptable voltage ever appears. If an unacceptable voltage does appear on the node, the user has the option to either continue or terminate simulation.
- Up to ten nodes in the circuit may be selected as the 'probe-points' of the simulation (output variables of the experimental frame). For these points, the transient response is calculated.

PDSE allows the user to define (or retrieve from a model data base) up to ten variations of any given model and ten different experimental frames. Once a set of models and experimental frames have been defined, the simulation process begins.

The experimental frame generator module produces waveforms that drive the circuit. The transducer observes voltage levels for each circuit probe point. If any of the node voltages from the simulation exceeds the maximum allowable voltage for that node in the circuit, the transducer signals this fact to the acceptor. The acceptor warns the user that one of the constraints for the simulation has been violated. At this point, the user has the option to continue or abort the simulation. If the user chooses to abort, or if all simulations are complete, the generator is disabled and the simulation halts.

This approach to managing the simulation process facilitates high flexibility in specifying design model alternatives and simulation experiment options. Through the notion of model and experimental frame bases, our simulation framework promotes reusability of model components in design studies and thus reduces the time to develop new models. The separation of experimental frames and models allows for comparative evaluation of several design alternatives with respect to a set of different design performance criteria.

3.3 Data Analysis and Post Processing

PDSE was designed to help the user understand the results of package simulations and apply those results to improve the package design. Currently, there are two sets of results available through PDSE once a set of simulations is complete. A graphics display window is provided to display the probe voltages resulting from the simulation of any one model and experimental frame input at one time. The display allows the user to quickly plot the results from other models or experimental frame inputs. It also features automatic scaling, zoom and pan features, and a cursor position display. A second window provides a numeric display of each of the nodes of a given model and simulation that had a voltage larger than the maximum allowable voltage.

These features aid the designer to evaluate various models. Other questions that may be answered by the appropriate analysis of the data are: "What is the settling time on line x?," "Do the voltages on line x monotonically cross some window threshold," "What is the voltage steady-state error on line x?". Knowledge based evaluation procedures are being incorporated in PDSE which will help in answering the types of questions stipulated above.

3.4 Interface Facilities

PDSE provides a robust, user-friendly shell integrating the processes described in the foregoing sections. We have developed pop-up menus, dialogue boxes, graphical I/O windows, based on the X-Windows package. We are currently interfacing PDSE with CAD data bases so that we can extract the interconnect description from a universal file format. This minimizes the labor intensive human interaction in inputting geometries. The IGES (Initial Graphics Exchange Specification) has been selected for this project. It is widely used in industry and is supported by the National Bureau of Standards [11].

The simulation tools embedded in PDSE impose restrictions on the types of interconnect systems that may be modelled. Due to those limitations, several assumptions have been made which simplify the data extraction algorithms. We do not allow tapered lines of tapered spaces between the lines. No line may branch into two lines nor are vias allowed. Conductors are represented in two-dimensional space. The conductor thickness is required but it is assumed to be constant throughout the length of the conductor [11].

The interconnect description is read from a CAD tool data base. No relationship between any two lines is assumed based on th order of descriptions found in the data base. Relationships between lines are found by the end points (the two sets of x,y coordinates that describe the line). Two lines that are connected have the same end points. Based on this information, we create graph structures. Once all data pertaining to the lines' description have been read, there exists one graph structure for every conductor in the system. After the graph structures have been created, the layout is displayed on the terminal and the designer is prompted to identify sections that will be considered for the coupled-line analysis. We have added capabilities to extend the 2-dimensional representation to the 3-dimensional one. A cross section of the selected conductor is automatically read by PDSE. The selected section serves as input geometry to PDSE's parameter extractor tools, i.e., UAC and UAMOM.

4. Support of Package Design Cycle

The long term objective of PDSE development is to employ system design, artificial intelligence, and simula-

tion/modeling techniques to support VLSI packaging design. PDSE will support activities of the design cycle as follows: The layout/routing, driver and receiver data will be obtained by accessing and/or editing and modifying the design data base. The layout will be translated into a geometrical representation. This representation will serve as an input to simulation tools. The simulation tools are used with appropriate experimental frames to generate performance measures for models (layouts) under consideration. Simulation output will be analyzed, and if problems exist, the layout will be edited and simulations will be re-run for a new model. This process, supported by our tools and appropriate knowledge bases, is shown in Figure 2 and is explained in more detail below.

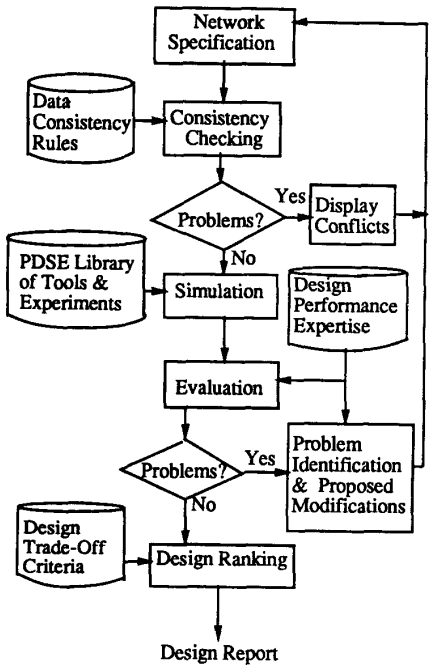

Fig. 2 Support of Package Design Cycle

A simulation run is set up using the library of simulation tools and experimental frames. Prior to applying an experimental frame to a design model, checks are made to ensure data consistency and validity. This requires that a rule base containing knowledge about data ranges, limits, etc. be invoked. We have implemented a prototype data consistency checker that performs the following functions: When UACSL or UANTL is to be executed, PDSE verifies that there are capacitance and inductance matrices provided for each transmission line system. If they have not been provided, PDSE automatically runs UAMOM or UAC to calculate these values. PDSE then looks for any short circuits or open circuits in the termination networks provided by the user. When the circuit components are input by the user, two node numbers are also input to specify the location in the network the component is to be placed. If any component has two node numbers which are the same, the user is notified of a short in the circuit. If throughout all the component specifications a node is only given once, an open circuit exists and, again, the user is notified of the situation. After all the data have been input and verified, the simulation process begins.

When executing UAMOM or UAC, PDSE verifies that all the geometry specifications outlined in Section 3.1 are satisfied. If any of these conditions are not satisfied, the user is prompted to correct the situation before continuing. There are several requirements that, if not satisfied by the user, can easily be corrected by PDSE. For example, both UAMOM and UAC require the conductor vertices be input in counter-clockwise order. If this has not been done, PDSE will correct the situation and continue with simulation. If the number of subintervals per side and the discretization are not specified, PDSE will assign default values and continue.

The simulation run will be constrained and channeled by design techniques and expertness built into the PDSE. Simulation results will be sieved by invoking a knowledge base of design expertise. Such a knowledge base will have to be constructed from results of research into design techniques and by eliciting information from literature and packaging experts. This knowledge will serve as a basis for determining whether the results of simulation studies are plausible or if they violate fundamental design performance expectations. If the results are not satisfying, the user will be able to use a scratch-pad editor to modify the layout and its parameters and re-run the simulation experiments.

To select the best possible design given often conflicting objectives (e.g., maximum performance vs. low cost), procedures must be developed for ranking alternative design models with respect to a set of performance measures. This will be accomplished by incorporating in PDSE trade-off procedures that will employ multiple-criteria decision making methods.

This is a conceptual framework in which PDSE offers design support. In summary, this will be accomplished by providing mechanisms for selecting a model representation given a design data base. The selection process will be driven by design constraints and objectives expressed using production rules. Models of designs will be evaluated in experimental frames using available simulation tools. A knowledge base of design expertise will be invoked to evaluate simulation results. If they violate fundamental design performance expectations, a model will be modified. There will be facilities for selecting satisfying design solutions given multiple design performance objectives.

5. Summary

PDSE is an integrated environment for modeling and simulation of the electrical characteristics in VLSI packages.

Users are able to efficiently simulate several variations of an interconnect package design in varying experimental conditions. The results of these simulations can be analyzed for selection of alternatives best satisfying design criteria.

PDSE is being integrated with computer automated design (CAD) tools. It will be able to directly read interconnect layout information from the CAD tool netlists, analyze the input from the netlist, and guide the user to improved design choices. This provides a strong foundation for building knowledge-based tools to support the package design cycle.

Acknowledgment

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