Computer Aided Design System for VLSI Interconnections

J. W. Rozenblit, J.L. Prince, O.A. Palusinski, and T.D. Whipple

Department of Electrical and Computer Engineering
University of Arizona
Tucson, Arizona 85721

Abstract

The paper describes a simulation environment for prediction of electrical characteristics of integrated circuit packaging structures. The simulation shell, Packaging Design Support Environment (PDSE), integrates tools for modeling and simulation of electrical characteristics in VLSI packages. They also provide facilities for supporting design of VLSI packages. Two simulation tools model inductance and capacitance for multiconductor, multidielectric, two-dimensional structures with lossy dielectrics. Another accepts the L and C matrices and computes pulse response characteristics of uniform multiple, coupled, lossless transmission lines which are terminated at discrete points with R, L, and C elements. The design process in PDSE proceeds in three major phases: modeling, simulation, and evaluation. These processes are interactive and allow the designer to refine a design model, modify simulation experiments, and apply various evaluation procedures.

1. Introduction

Advances in semiconductor technology have brought about a dramatic increase in speed of operation of silicon devices and integrated circuits. As signal rise times become shorter than 1 ns, the electrical performance of interconnections becomes an important factor in the engineering design. There are many electromagnetic phenomena that are becoming important in determining the signal integrity and overall system performance at such speeds. The behavior of interconnections has become an important issue in VLSI packaging because of the "crosstalk" and reflections which increase as the density of packaging becomes higher and the distance between adjacent conductors becomes smaller.

The problem of predicting the performance of interconnections is very complex and the use of modeling techniques and computer simulation of interconnecting structures is necessary. The simulation of transients in the interconnections is a principal way of obtaining information about the electrical performance of the designed system. Experimentation with hardware and its subsequent redesigning-remanufacturing is very expensive in terms of time, materials, and use of equipment, and as such is not practical. This reinforces the significance of simulation and relevant supporting software.

Our methodology for supporting VLSI package design is derived from the model-based system design framework developed by Rozenblit [1] [2]. In this methodology, the designer develops a model from which a new system will be created. As opposed to system analysis, where the model is derived from an existing, real system, in design the model comes first as a set of "blueprints" from which the system will be built, implemented, or deployed. The blueprints might take several forms; they could be simple informal descriptions, a set of equations, or a complex computer program. The goal of the model-based design methodology is to study models of designs before they are implemented and physically realized.

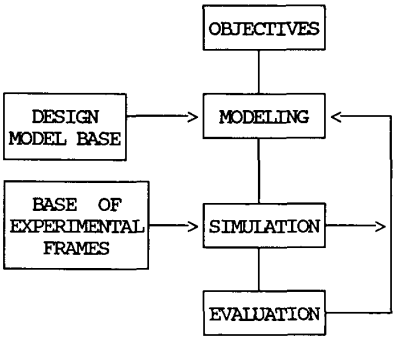

Figure 1. Design in the modeling context.

As depicted in Figure 1, the design process is supported by the methodology as follows: Design Objectives (understood here as a set of design requirements, constraints, and purposes for which a design process is undertaken) drive the design model development process. In this process the designer has facilities for retrieval of design models which conform to the objectives, constraints, and requirements from the Design Model Base. If no models can be retrieved, a new model is constructed. It is assumed that all

possible design models that satisfy design constraints and requirements are generated. They are termed design alternatives. The models are then evaluated through simulation studies. To carry out a simulation run, an experimental frame, i.e., the set of circumstances under which a model is observed [3], must be defined. Again, the designer may retrieve an appropriate experimental frame from the Base of Experimental Frames or define a new one. The simulation phase is followed by evaluation of the results and ranking of design alternatives. The alternatives are ranked with respect to experimental frames under which simulation runs have been performed. Thus, design models whose performance conforms best to the design objectives are selected as a basis for design implementation.

Notice that the separation of models and corresponding experiments, as well as the model and experiment base approach, results in reusability of design models/experiments and high flexibility in evaluating alternative designs. This approach is the basis for design of the Packaging Design Support Environment.

2. Packaging Design Support Environment (PDSE)

Our research and development work has focused on integrating the modeling and simulation modules developed under our VLSI Packaging and Interconnection Program into an electronic packaging design support software. This software, called Packaging Design Support Environment (PDSE), integrates existing electrical (and eventually thermal/mechanical) software modules for VLSI package simulation and provides facilities for supporting design of VLSI packages. The individual modules are embedded in an interactive software environment implemented on a DEC VAXstation II/GPX under the Ultrix-32 operating system.

Figure 2 depicts the functional levels of PDSE's design. The lowest level is currently comprised of the electrical simulation modeling tools. Facilities for the design model and experimental frame specification are provided at Level 1. The Simulation Management level has tools for model and experiment selection, initialization of simulation runs, and handling of data storage. Level 4, still under development, will include knowledge bases with expertise for analysis of simulation data, validation of results and support in design model selection. The User Interface supports the user/system dialogue.

Level 4: User Interface.
Level 3: Expertise & Post Processing.
Level 2: Simulation Management.
Level 1: Model & Experimental Frame Specification.
Level 0: Simulation Tools.

Figure 2. Functional Levels of PDSE.

We now proceed to describe these design levels in more detail.

2.1 Electrical Modeling and Simulation Tools

A typical interconnection system can be decomposed into terminating networks, sections of multi-conductor parallel lines, and discontinuities (bends, junctions, cross-overs, vias). The terminating networks are modelled utilizing lumped parameter equivalent circuits for the components like transistors, independent sources, and R, L, C elements. The mathematical models of networks are determined using well established circuit analysis techniques. The sections of multi-conductor parallel interconnections are modelled as multi-wire transmission lines described by one-dimensional wave equations. The discontinuities are replaced by their lumped parameter equivalent circuits [4]. Several tools have been developed to simulate the transients on such interconnect systems.

Coupled Line Simulator (UACSL) [5] is a tool that will simulate the transient response of a general linear network containing resistors, conductors, capacitors, inductors, coupled inductors, piecewise linear independent voltage sources, and lossless uniform transmission line systems. Up to 50 independent voltage sources, 10 transmission line systems, and 100 of each type of component may be specified. Each transmission line system can be composed of up to ten conductors and must be described by their length and by the capacitance and inductance matrices as calculated by one of the parameter calculators described below.

Method of Moments TEM Transmission Line Parameter Calculator (UAMOM) [6] and UA Capacitor Calculator (UAC) [7] will calculate the capacitance and inductance matrices (per unit length) of a parallel multiconductor transmission line system given its cross-sectional geometry. Lines are assumed to be of infinite length, and end effects are not calculated. Ground planes and dielectric interfaces are taken as infinite in extent. Up to ten conductors may be specified, and each conductor may have up to twelve sides. The specific limitations of each tool are described in the sections below.

For UAMOM, up to six dielectric layers may be specified. The moment calculator will evaluate the TEM line parameters for geometries that lie in one of the categories below:

1. One infinite ground plane present (microstrip-like)
2. Two infinite ground planes present (stripline-like)
3. Only finite sized ground conductors present.

Up to ten arbitrarily shaped conductors may be defined, any number of which may designated as

ground conductors. Conductors may intersect with any number of dielectric interfaces, but must not touch each other or ground planes. To facilitate the calculation of the parameters, all of the conductor sides and dielectric interfaces are approximated by straight line segments (subintervals.) The more subintervals per side, the longer the calculation will take. The dielectric interfaces and ground planes must be truncated at a fixed distance from the conductors.

The allowable geometries for UAC are more limited than those allowed for UAMOM. These geometries are described below:

1. One finite ground conductor, no ground planes, two dielectric layers.
2. One infinite ground plane, no finite conductors, two dielectric layers.
3. Two infinite ground planes, no finite conductors, one dielectric layer.

In each case every conductor must lie wholly within one dielectric medium. Conductor placement is arbitrary as long as the conductor does not touch any ground plane or dielectric interface. As in UAMOM, the number of subintervals per side may be specified for the calculation.

2.2 Model and Experimental Frame Specification

As mentioned in Section 1, the separation of model and experiment is the basis for managing the simulation studies in PDSE. The experimental frame concept is used to simulate several variations of a model with several variations of input to the model [8]. This is illustrated in Figure 3.

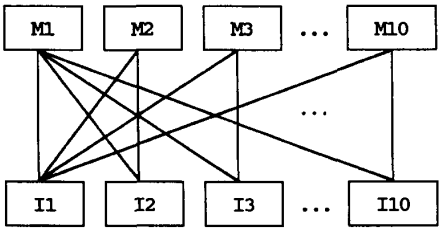

Figure 3. Block diagram of multiple-model, multiple-input simulation.

There are three steps in performing a coupled line analysis in PDSE -- create the model(s), define the experimental frame, and run the simulation. This section describes the model and experimental frame specification.

PDSE allows the user to define (or retrieve from a model data base) up to ten variations of any given model. When the user selects the 'create models' option, a 'circuit specifications' menu appears. Through this menu, resistors, capacitors, inductors, coupled inductors, voltage sources, and transmission line systems may be specified. Each of the components are specified by its connecting node numbers and component value (resistance, capacitance, etc.) To specify a transmission line system, all that is needed is the connection node numbers, transmission line length, and its cross-sectional geometry. These data are all input through a graphical, spread-sheet like user interface. Up to ten nodes in the circuit may be selected as the 'probe-points' of the simulation -- those points for which the simulation results are calculated.

The experimental frame is defined independently of the models. It consists of a set of input waveforms for each voltage source defined in the model and control variables (which allow the user to monitor the simulation.) Up to ten waveforms may be defined. The waveforms may be defined as a set of step inputs with a range of up to ten different rise times, or may be a set of up to ten generic waveforms defined by piecewise linear segments. There are two sets of control variables which must be defined. First is the simulation length. The second is a set of maximum allowable voltages for each probe point in the circuit. This allows the user to monitor each probe point to know if an unacceptable voltage ever appears. If an unacceptable voltage does appear on the node, the user has the option to either continue or terminate simulation.

2.3 Simulation Management

Once a set of models and an experimental frame have been defined, the simulation process may begin. Management of the simulation process is illustrated in Figure 4.

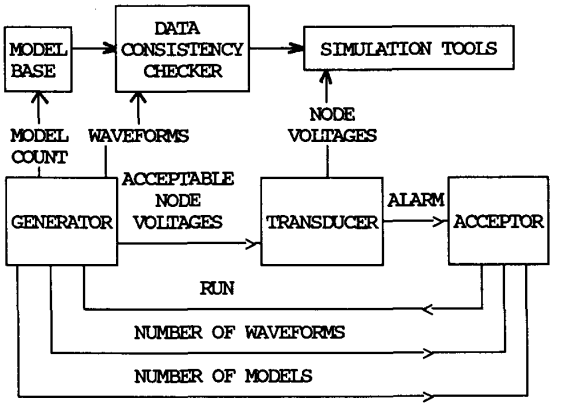

Figure 4. Block diagram of coupled-line analysis experimental frame.

As long as the Run line (from the Acceptor) is enabled, the Generator generates waveforms for the Data Consistency Checker, identifies which model is to be simulated, and informs the Transducer of the acceptable voltage level for each circuit probe. It also signals the Acceptor how many waveforms and models there are in the simulation. The Transducer gathers output from the simulation tools. If any of the node voltages from the simulation exceed the maximum allowable voltage for that node in the circuit, the Transducer signals this fact to the Acceptor through the Alarm. The Acceptor monitors the Alarm line and the simulation count. If the Alarm line is set, the Acceptor warns the user that one of the constraints for the simulation has been violated. At this point, the user has the option to continue or abort the simulation. If the user chooses to abort, or if all simulations are complete, the Run signal to the generator is disabled and simulation halts.

The Data Consistency Checker has been designed so that inconsistent or missing data will be automatically replaced when possible. When this is not possible, the user is informed about the problem, and the simulation process is not started until the discrepancy is corrected.

When UACSL is to be executed, PDSE verifies that there are capacitance and inductance matrices provided for each transmission line system. If they have not been provided, PDSE will automatically run UAMOM or UAC to calculate these values. PDSE then looks for any short circuits or open circuits in the termination networks provided by the user. When the circuit components are input by the user, two node numbers are also input to specify the location in the network the component is to be placed. If any component has two node numbers which are the same, the user is notified of a short in the circuit. If throughout all the component specifications a node is only given once, an open circuit exists and, again, the user is notified of the situation. After all the data has been input and verified, the simulation process begins.

When executing UAMOM or UAC, PDSE verifies that all the specifications outlined in Section 2.1 are satisfied. If any of these conditions are not satisfied, the user is prompted to correct the situation before continuing. There are several requirements that, if not satisfied by the user, can easily be corrected by PDSE. For example, both UAMOM and UAC require the conductor vertices to be input in counter-clockwise order. If this has not been done, PDSE will correct the situation and continue with simulation. If the number of subintervals per side and the discretization in x are not specified, PDSE will assign default values and continue.

2.4 Design Expertise and Post Processing

Currently, there are two sets of results available through PDSE once a set of simulations is complete. A graphics display window is provided to display the probe voltages resulting from the simulation of any one model and model input at one time. It also allows to switch quickly to the plots of results from other models or other model inputs. The window features automatic scaling, zoom and pan features, and a cursor position display. A second window provides a numeric display of each of the nodes of a given model and simulation that had a voltage larger than the maximum allowable voltage.

These features aid the designer as the designer attempts to evaluate various models. It is planned, however, to add knowledge based evaluation procedures to PDSE which will evaluate the simulation results and rank the models based on various design criteria. Not only will PDSE rank design models, but it will offer suggestions on how to improve designs. The models can then be modified, re-simulated, and re-evaluated. This concept is further discussed in Section 3.

2.5 User Interface

PDSE provides a robust, user-friendly shell integrating the processes described above. We have developed pop-up menus, dialogue boxes, graphical i/o windows, and spread sheet windows based on the X-Windows graphics package to accomplish this.

3. Support of Package Design Cycle

The long term objective of PDSE development is to employ system design, artificial intelligence, and simulation/modeling techniques to support VLSI packaging design. PDSE will support activities of the design cycle as follows: The layout/routing, driver and receiver data will be obtained by accessing and/or editing and modifying the design data base. The layout will be translated into a geometrical representation. This representation will serve as an input to simulation tools. The simulation tools will be used with appropriate experimental frames to generate performance measures for models (layouts) under consideration. Simulation output will be analyzed, and if problems exist, the layout will be edited and simulations will be re-run for a new model. This process is shown in Figure 5 and is explained in more detail below.

A simulation run will be set up using the library of simulation tools and experimental frames. Prior to applying an experimental frame to a design model, checks will be made to ensure data consistency and validity. This will require that a rule base containing knowledge about data ranges, limits, etc. be invoked. The simulation run itself will be constrained and channeled by design techniques and expertness built into the PDSE.

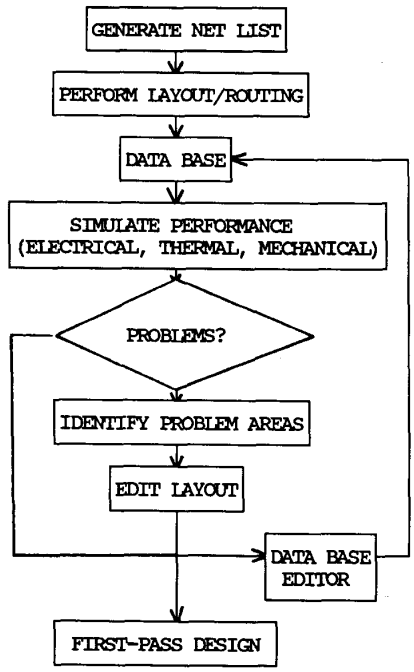

Figure 5. PDSE Design Cycle.

Simulation results will be sieved by invoking a knowledge base of design expertise. Such a knowledge base will have to be constructed from results of research into design techniques and by eliciting information from literature and packaging experts. This knowledge will serve as a basis for determining whether the results of simulation studies are plausible or if they violate fundamental design performance expectations. If the results are not satisfying, the user will be able to use a scratch-pad editor to modify the layout and its parameters and re-run the simulation experiments.

To select the best possible design given often conflicting objectives (e.g., maximum performance vs. low cost), procedures must be developed for ranking alternative design models with respect to a set of performance measures. This will be accomplished by incorporating in PDSE trade-off procedures that will employ multiple-criteria decision making methods.

This is a conceptual framework in which PDSE will offer design support. In summary, this will be accomplished by providing mechanisms for selecting a model representation given a design data base. The selection process will be driven by design constraints and objectives expressed using production rules. Models of designs will be evaluated in experimental frames using available simulation tools. A knowledge base of design expertise will be invoked to evaluate simulation results. If they violate fundamental design performance expectations, a model will be modified. There will be facilities for selecting satisfying design solutions given multiple design performance objectives.

4. Summary

PDSE, as described in the previous sections, provides a user-friendly environment for modeling and simulating the electrical characteristics in VLSI packages. The experimental frame facilitates the evaluation of various package design models. Users are able to efficiently simulate several variations of an interconnect package design based on varying inputs. The results of these simulations are graphically displayed. This allows the user to easily make design choices based on the simulation results.

PDSE will eventually be integrated with computer automated design (CAD) tools. It will then be able to directly read interconnect layout information from the CAD tool netlists, analyze the input from the netlist, and guide the user to improved design choices. This provides a strong foundation for building knowledge-based tools to support the package design cycle mentioned in Section 3.

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