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DESIGN ARTICLE

A knowledge-based simulation environment for the early design of multichip modules

P.Hsu†, R. Senthinathan*, J. W. Rozenblit†, and J. L. Prince†.
†Center for Electronic Packaging Research, Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ 85721, U.S.A.
Tel: [1] (602) 621-6177. Fax: [1] (602) 621-8076.

* IBM: E. Fishkill Semiconductor Laboratory, Electrical Package Integration, Hopewell Junction, NY 12533, U.S.A.

A knowledge-based simulation environment is developed to facilitate the early design of Multichip Modules (MCMs). Electrical system performance measures such as module clock frequency, etc. are predicted and analyzed for different interconnect and packaging technologies. Performance-limiting factors such as power dissipation, coupled noise, and simultaneous switching noise are also included in this work. CMOS based MCMs for workstation applications are used to demonstrate the feasibility of the system in development.

1. INTRODUCTION

Multichip Modules (MCMs) which shorten the average interconnection length by eliminating the individual chip packages have had significant impact on the application of high performance electronics in recent years. Using this packaging technique, not only is the integration density increased, chip-to-chip delay is also significantly reduced. Thus the system performance such as module clock frequency is improved. Overall understanding of the trade-offs among different aspects of performance metrics such as electrical, thermal, material, reliability, is the key to the successful system design of MCMs [1] [2]. The goal is to maximize the performance to cost ratio so that system product is competitive in the market. Due to the high cost of manufacturing, processing, rework, and testing for MCMs, early estimation and evaluation of the system performance is especially essential before any physical design.

This paper emphasizes the electrical performance evaluation for MCM early design. The other matrices such as material, thermal, cost and reliability, *etc.* will be included in future work. Module clock frequency, module size, power dissipation, and noise to signal ratio (includes the considerations of crosstalk and simultaneous switching noise) are considered as electrical performance metrics in this work.

Because of the advantages of higher integration and lower power consumption, CMOS based implementation of multichip modules is selected for our discussion.

Usually the early system design of MCM is complicated by many trade-offs resulting from conflicting design constraints and performance goals set up by different companies due to their specific purposes and technological limits. To globally optimize all performance metrics, a designer has to consider a large number of design parameters, their interdependencies and trade-offs simultaneously.

For example, higher system clock frequency usually requires higher chips integration and proper interconnect/package technologies. However, higher module frequency and chip integration increase the power

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dissipation. Due to the noise to signal ratio, crosstalk and simultaneous switching noise might limit the level of chip integration and interconnect technology used, thereby higher module frequency might not be able to be achieved for a given MCM design.

The dependencies among the design parameters might be complex in one sense, but are very important and useful especially to the decision making of early MCM system design. In such a decision making process, a designer usually has to rely on different kinds of knowledge about his task domain. A system that can integrate different kinds of knowledge to effectively support user's activities during design cycle is desirable.

In this work, a knowledge-based simulation environment is developed to facilitate the performance evaluation of early MCM design. The system provides useful information regarding the dependencies among the design parameters. The information can be used as a guide in searching for a better solution and to gain insight into the nature of the design problem's solution space.

Selected detailed simulations can then be used for further analysis. The overall concept is illustrated in Figure 1. MCM conceptual design is our domain. The lower two oval-shaped regions can be considered as our solution spaces. The detailed simulation tools in the figure mean rigorous electromagnetic full-wave analysis

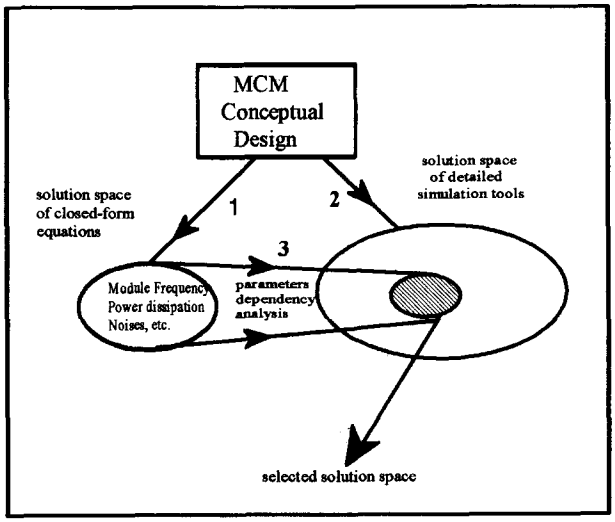


Figure 1: Three different approaches for MCM early design.

tools for electrical parasitic extractions or waveform simulations. The performance metrics estimated by closed-form equations (approach 1) might not be numerically accurate, but are good for rapid design space evaluation. Furthermore, the overall picture of the system performance can be easily captured by this scheme.

The system designers can investigate the trade-offs and interdependencies among design parameters more efficiently. Detailed simulation tools (approach 2) are necessary for the assessment of electrical performance characteristics of a pre-selected candidate MCM but are usually computationally expensive. Besides, it is difficult to predict the dependencies among design parameters and performance trends by just one or two simulations.

In this work, a trade-off approach (approach 3) is adopted for MCM early design: closed-form equations are used for global analysis; detailed simulation tools are used for local analysis. The "knowledge" obtained from the solution space of closed-form equations is used to guide the system designer in selecting appropriate simulations for further analysis using detailed tools.

The features of this proposed simulation environment under development are summarized as follows:

- *Evaluation.* One obvious, elementary function of the environment is to evaluate the set of constraints for given values of known parameters. This ability is essential to enable the designer to examine the basic relationships and trade-offs between design parameters.

- *Minimization of computation.* Simulation techniques are essential for performance evaluation of the early system design, however, detailed simulations can be computationally expensive. During evaluation, the expensive calculations should be minimized. Detailed simulations must be applied only to the design space with localized interests. In this work, several fast and reliable closed-form equations are established for performance estimation and dependency analysis. By applying these equations, computational effort is significantly reduced.

- *Flexibility.* In order to realize such an environment, heterogeneous knowledge sources need to be included in a system. The system's flexibility and expansibility must be assured so that new knowledge sources can be easily updated and included. Currently the simulation environment includes detailed simulation tools, closed-form equations, prior designs, MCM model base for simulations, CAD interconnect layouts, look-up tables, as knowledge sources.

In the next section, the MCM system model and the corresponding closed-form equations for performance estimations are described. We discuss in detail the architecture of the knowledge-based simulation environment and how this system is used to evaluate the electrical performance for early MCM system design in section III. Examples are given. In the last two sections, we survey the related work and discuss future directions.

II. MCM MODELS

In the following sub-sections, a first-order equivalent circuit model of MCM is presented; Closed-form equations for predicting and estimating the module frequency, module size, power dissipation, and simultaneous switching noise are also described. Closed-form equations for other performance estimations will be included in the future.

2.1 Equivalent Circuit and Module Size

The equivalent MCM circuit for calculating the system clock frequency is shown in Figure 2, where $Rd_{out}(\Omega)$ is output driver resistance, $C_{pad}(pF)$ is bond pad capacitance, $V_{in}(t)(V)$ is the driving voltage source, $R_{int}(\Omega/cm)$ is per unit length (p.u.l.) interconnect resistance, $C_{int}(pF/cm)$ is p.u.l. interconnect capacitance, $C_{rec}(pF)$ is the input capacitance of a receiver, and f_o is the fanout of the output driver (for example, $f_o = 3$ in Figure 2). R_{int} is included before the off-chip inter-connect for the consideration of losses, although in detailed model, this value is distributed along the interconnect.

In this work, it is assumed that the width and length of the MCM are of equal dimension. For the calculation of interconnect length $L_{int}(cm)$, the worst case chip-to-chip delay path is assumed by calculating the dimension of the module twice:

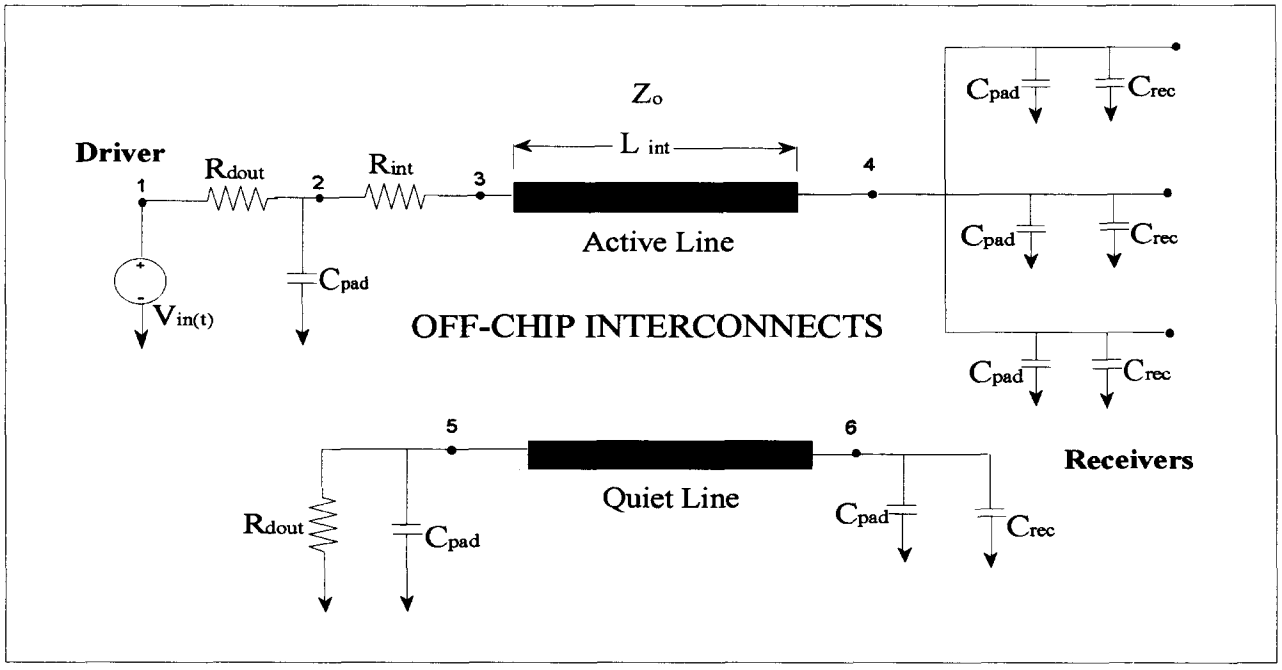


Figure 2: An equivalent MCM circuit model for analysis.

$$L_{int} = 2\sqrt{F_p\ Nc}, \qquad (1)$$

where F_p (cm^2) is the footprint size of a logic chip, which is limited by module wiring capacity and bond pad, and Nc is the total number of "equivalent chips" in an MCM. Usually in a multichip module, there are logic chips and memory chips. The size (chip area) of memory chips is different from logic chips. The number of "equivalent chips" is defined here as the number of "equivalent logic chips", and this term will be used for the rest of the discussions.

If P is the total number of logic chips, Q is the total number of memory chips in a multichip module, and ζ is average chip size (area) ratio between logic and memory chips integrated onto the module, then the number of equivalent chips (N_c) is:

$$N_c = (P + Q/\zeta). \qquad (2)$$

The module size M_{size} (cm^2) can then be estimated as:

$$M_{size} = N_c F_p \qquad (3)$$

2.2 Module Frequency

Initial work on module frequency estimation for systems is given by Bakoglu [3]. In this work, some of the equations are modified especially for CMOS-based systems. These equations are listed and described below.

Cascaded drivers (inverter chains) are applied in the system model because of the consideration of large fanout in MCM application. The driving-chip (on-chip) delay T_c can be calculated from:

$$T_c = \frac{1}{f_c} + 2e(N-1)R_{tr}C_{tr} \times 10^{-15}\ \text{sec} \qquad (4)$$

where f_c is chip operating frequency in an MCM, and e+(e=2.71...) is the optimal ratio of two consecutive drivers. $R_{tr}(\Omega)$ and $C_{tr}(fF)$ are the ON-resistance and input capacitance of a minimum-sized nMOS and pMOS transistors, (i.e. R_{tr}(nMOS) is equal to R_{tr}(pMOS)). The number of stages N can be calculated by setting the ON-resistance of the output stage to Z_0 (off-chip interconnect characteristic impedance) and pessimistically assuming that the first inverter of the cascaded chain is a minimum-sized device:

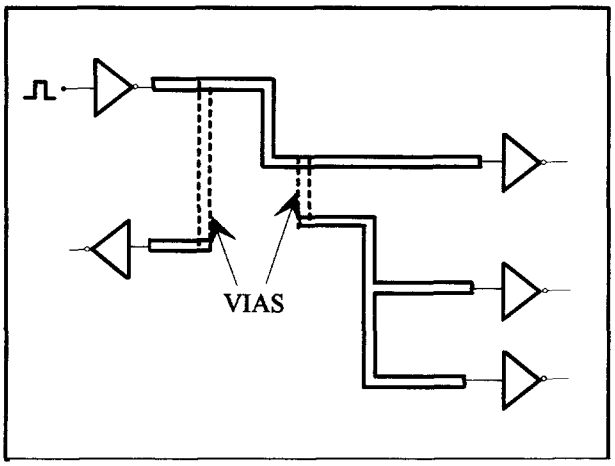


Figure 3. Interconnect structure with bends and vias.

$$N = 1 + ln\left(\frac{R_{tr}f_0}{Z_0}\right). \qquad (5)$$

In addition to chip delay T_c, RC delays (T_{m1} to T_{m5}, as shown below) which consider the charging/discharging of the driver, receivers and interconnect capacitance, and transmission line propagation delay T_{m6} need also to be included for the module delay calculation.

$$T_{m1} = (1 + f_0)(C_{pad}R_{dout}) \times 10^{-12}\text{sec}, \qquad (6)$$

$$T_{m2} = \frac{1}{2}(R_{int}L_{int})(C_{int}L_{int}) \times 10^{-12}\ \text{sec}, \qquad (7)$$

$$T_{m3} = R_{dout}(C_{int}L_{int})f_0 \times 10^{-12}\text{sec}, \qquad (8)$$

$$T_{m4} = R_{dout}C_{rec}f_0 \times 10^{-12}\text{sec}, \qquad (9)$$

$$T_{m5} = R_{int}L_{int}C_{rec} \times 10^{-12}\text{sec}, \qquad (10)$$

$$T_{m6} = \frac{L_{int}}{V_m} \qquad (11)$$

where V_m is the propagation velocity. Notice that these equations also include bond pad parasitics and consider the effect of fan-outs for CMOS implementation. The module frequency M_f(MHz) can then be calculated as:

$$M_f = (T_c + \sum_{i=1}^{6} T_{mi})^{-1} \quad (12)$$

Since our simple model forms a RC tree like network, to determine the delay with higher accuracy on a specific branch, one needs to calculate the contribution of each other branch on the branch of interest for this RC tree. Detailed analysis on the calculation of delay using RC tree approach is given in [4]. In this application, calculated interconnect length L_{int} is adopted only when the error of off-chip delay is within 10% when compared with that determined by detailed tools.

Also note that, with stub-like loading, bends and vias (in Figure 3), our simple approach will give more than 25% error for long interconnect length, and more detailed simulations are essential to predict the maximum module frequency.

2.3 Power Dissipation

Power dissipation of an MCM can be calculated from:

$$M_{power} = 1/2\, F_D M_f C_m V_{DD}^2, \quad (13)$$

where F_D is the percentage of the lines that switches, M_f is the module clock frequency, and C_m is the total capacitance related to chip-to-chip lines, including both the interconnection and gate capacitances of the output buffers and the pad capacitances. The total module capacitance is thus:

$$C_m = [(1+f_0)C_{pad} + 2\,\frac{1-e^N}{1-e}\,C_{tr} + \sqrt{F_p R_M C_{int}}]N_c N_{I/O}, \quad (14)$$

where $N_{I/O}$ is the estimated number of I/O's per chip which is determined by the Rent's rule and R_M is the average interconnection length at the module level in units of chip pitches, which is calculated using Rent's and Donath's [5, 6] equations as:

$$R_m = \frac{2}{9}\left(7\,\frac{N_c^{\eta-0.5}-1}{4^{\eta-0.5}-1} - \frac{1-N_c^{\eta-0.75}}{1-4^{\eta-0.75}}\right)\frac{1-4^{\eta-1}}{1-N_c^{\eta-1}} \quad (15)$$

where η is the Rent's constant for package level interconnection. and N_c is the total effective number of chips on the module.

2.4 Simultaneous Switching Noise for CMOS-based MCMs

Increase in density and switching speed increases the Simultaneous Switching Noise (SSN). Even though output driver simultaneous switching is a repetitive event, at any given time the maximum peak SSN voltage must be less than the maximum allowable noise to avoid any false switchings. Detailed analysis on calculating the maximum allowable noise is explained using noise immunity characteristics of CMOS circuits [7]. A method of calculating SSN for CMOS-based systems are given in [8]. From [8], for n number of output drivers switching simultaneously, the maximum peak switching ground noise V_n is:

$$V_n = V_k + \frac{1}{L_{VSS}}\,\frac{1}{\sum_{i=1}^{n}\frac{K_i}{T_i}}\left[1-\sqrt{1+2\,V_k L_{VSS}\sum\frac{K_i}{T_i}}\right] \quad (16)$$

Here $K_i = \mu_n C_{ox}(W/L)$ for i^{th} N-channel output driver device, T_i is the time taken for the i^{th} current spike to travel from zero to its maximum peak value, and $V_k = V_{in} - V_t$. Here L_{VSS} is the effective chip-package lumped inductance as seen by the output drivers on their V_{SS} path. Note that, modeling L_{VSS} is complicated for MCMs, and require rigorous software tools. This is because there exits multiple current paths from the on-chip V_{SS} buses to the external ideal ground.

In addition to multiple current paths, currents also re-distribute on all the V_{SS} planes. It is essential to understand in detail the current paths, and their contributions to the over all L_{VSS} inductance network. Method of modeling L_{VSS} for a single chip package is given in [9], and a first-order L_{VSS} model for MCMs is explained in [11].

Consider a MCM with N number of chips each having q_i number of chip-package connections. In addition, there are m number of V_{SS} planes with adjacent V_{SS} planes strapped together with K_i number of via connections, and p number of pins connected to the bottom-most V_{SS} plane. From [11], the effective inductance "L_{VSS}" seen by the output driver is,

$$L_{VSS} \approx \frac{L_{c\text{-}p}}{\sum_{i=1}^{N} q_i} + \sum_{i=1}^{m-1} L^{i}_{plane}(K_i) + \sum_{j=1}^{m-1} \frac{L^{j,j+1}_{via}}{K_j} + L^{m}_{plane}(p) + \frac{L_{pin}}{p} \quad (17)$$

Here $L_{c\text{-}p}$ is the chip-package inductance for a single connection, L^{i}_{plane} is the inductance of the $i^{th}V_{SS}$ plane, $L^{j,j+1}_{via}$ is the inductance for a single via connection between planes j and j+1, and L_{pin} is the package-pin inductance for a single connection. A detailed frequency-independent package plane parasitic calculator was used to extract the plane inductance [12]. In this model, mutual inductance between planes are not included. However, for unevenly distributed via and pin connections on an MCM V_{SS} planes, mutual inductance between planes need to be incorporated in the L_{VSS} model. Note that N=1 with m=1 in the L_{VSS} calculation equation corresponds to a single chip with one V_{SS} plane connection. For workstation application MCM SSN calculations, the following number of simultaneously switching outputs (n) was selected [11].

$$n = \frac{1}{4}(\#\ of\ chips) x (data\ /\ address\ bus\ width) \quad (18)$$

Note that this is not a worst case, and represents a typical case where either the data or the address bus in 50% of the logic chips are switching from low-to-high or high-to-low at a given arbitrary time T.

Rent's rule with appropriate constants (k and β) for CMOS MCMs was used to calculate the total number of chip-package connections N_p,

$$N_p = 1.4\ (N_c \times N_{I/O})^{0.63} \quad (19)$$

N_c is the ``equivalent" number of chips and $N_{I/O}$ is the number of I/O's for each chip.

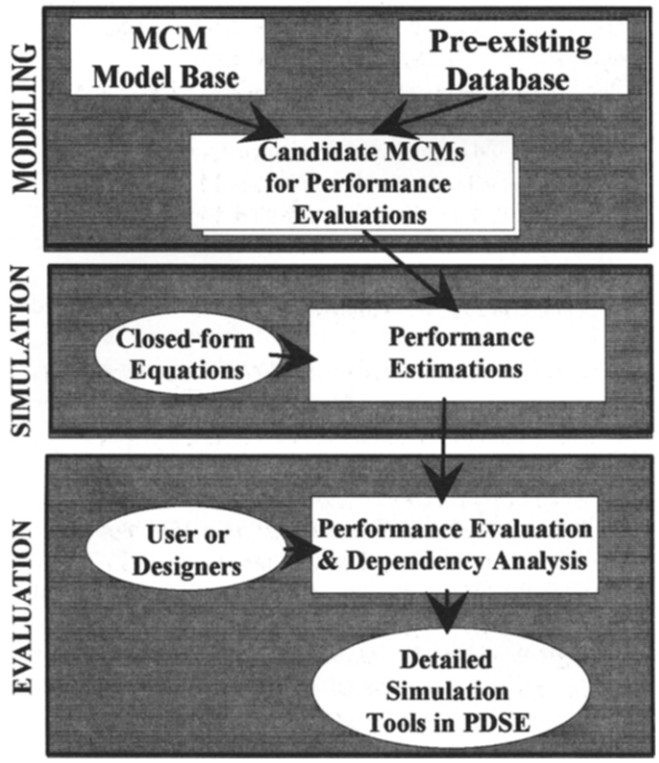


Figure 4. The system architecture for MCM performance analysis.

III. THE SIMULATION ENVIRONMENT

This section describes the architecture of the proposed simulation environment for MCM early design. The system consists of three different layers: *modeling, simulation and evaluation*, and the structure is shown in Figure 4. The knowledge-based simulation environment described here is implemented in C/C++ programming languages and running on UNIX based workstation. It is developed on top of an existing electronic packaging simulation environment called PDSE (Packaging Design Support Environment) [13].

PDSE is an X-Window based environment integrating many *detailed simulation tools* such as electrical parasitic extractors and waveform simulators which can be used to generate information on characteristic impedance, delay, attenuation, crosstalk and other relevant electrical performance characteristics for a given interconnect technology. Those detailed simulation tools can be applied as knowledge sources for MCM early design. Readers can refer to [14] for more information about the described software tools.

3.1 Modeling

We construct candidate MCM models for performance evaluation in the modeling layer. With varieties of design options (based on different technologies) available for MCM early design, on object-oriented paradigm and frames [15] are used to facilitate the organization and representation of the *knowledge* we have about MCM models. Object--oriented model base supports *data abstraction, inheritance,* and *run-time method determination.* Each feature helps to build more abstract, powerful, and malleable data types. The following *classes* are established to represent the attributes associated with an MCM:

- *Interconnect technology* This includes interconnect cross section geometry, thin film or thick film technology, stripline or microstrip line structure, substrate dielectric, conductor resistivity.
- *Logic technology* The characteristics associated with the CMOS output driver device and receivers, the supply voltage.
- *Chip technology* Number of logic chips, memory chips. The average chip size ratio between logic chip and memory chip. Chip's footprint size. Number of I/O's for each chip.
- *Bonding technology* Flip chip, wire bonding, or TAB (tape automated bonding).
- *Effective inductance* Chip-package inductance for a single connection, V_{SS} plane inductance, inductance for via connections, and package-pin inductance for a single connection.

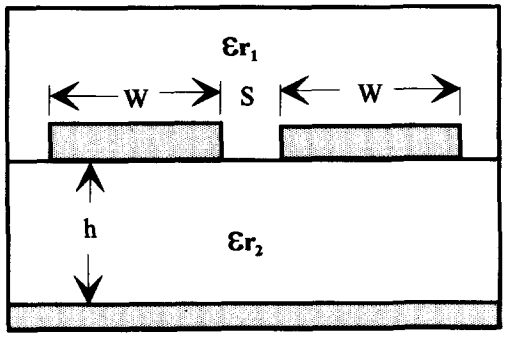
The construction of object-oriented conceptual model and application of frame-based knowledge representation not only make our model base for MCMs more modular, but make the generation of candidate MCM models for simulation and evaluation more easy and straightforward. New MCM models can be created through multiple inheritance from related base classes (set of attributes for MCMs). The addition of new classes (for example, we consider thermal attributes in the future) will not influence the current applications so that the expansibility of the current simulation environment can be assured.

The attributes of an MCM model can also be retrieved from the pre-existing database which is currently under active development. The pre-existing database contains information about prior MCM designs which satisfy certain constraints or some look-up tables. For example, look-up table with calculated plane inductances is very useful to study simultaneous switching noise with various V_{DD} / V_{SS} package pin placement.
This is because using detailed simulation tool such as UALGRL [12] to calculate those values is very time-consuming. The database can also include interconnect layout from a CAD graphic tool. MCM's interconnect geometry can be directly extracted for performance analysis [16].

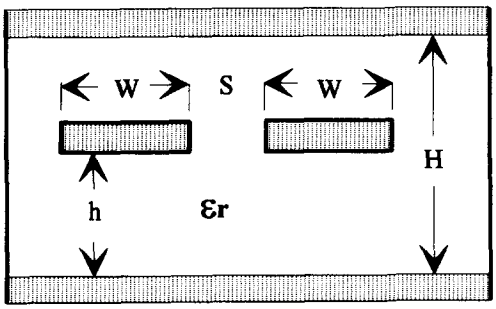
3.2 Simulation and Evaluation

Once the candidate MCM models for performance evaluation are available, simulation can proceed. We calculate the MCM performance metrics by invoking the close-form equations derived in section II. Because the values of parameters in different candidate MCMs vary, design curves for the dependencies between performance matrices and parameters concerned can be plotted quickly for analysis. Note that such curves might take even longer to generate if only detailed simulation tools are involved for calculations. The performance trends predicted by the set of design curves are the preliminary evaluation results provided by the system.

The design curves are used to guide the MCM designers to look into the problem of his original conceptual design space. System designer has to involve after this stage to utilize (interact with) the "solution space" which is set of design curves provided by the system in



(a) Microstrip lines cross section.



(b) Strip lines cross section

Figure 5. The cross section of two different interconnect structures.

order to gain better insight into his original conceptual design.

Design trade-offs can also be investigated through examining the trends predicted by the system. The satisfactory MCM configuration can then be selected and localized for further detailed analysis by interfacing with the electromagnetic full-wave simulation tools integrated in PDSE.

3.3 Examples

Cases for MCM's application on a workstation are presented in this subsection, however the methodology mentioned in the last subsection can be applied to other MCM application. Listed below is the information of candidate MCMs for performance evaluation.

- *Interconnect technology*: Two interconnect structures: strip line and microstrip line are considered for both thin film and thickfilm technologies. The typical interconnect cross sections for these structures are shown in Figures 5a and 5b. The dimensions of the cross section geometry selected for study are: 1) thin film microstrip line, w=10μm, t=2μm, h=10μm; 2) thin film strip line, w=10μm, t=2μm, h=10μm, H=20μm; 3) thick film microstrip line, w=3 *mil*, t=1 *mil*, h=10 *mil*; 4) thick film strip line,w=3 *mil*, t=1 *mil*, h=10 *mil*, H=20 *mil*. Relative permittivity ε_{r1} for the microstrip line structure is equal to the permittivity of free space, which is 1. The value of ε_{r2} for microstrip line, and that of ε_r for strip line case are selected based upon the availability and feasibility and range from 2.5 to 11.7. Copper is selected as conductor material with resistivity ρ = *1.7 Ω. cm.*

- *Logic technology*: The values of ON-resistance R_{tr} and input capacitance C_{tr} of a minimum-sized nMOS/pMOS transistors (smallest pre-driver of the cascaded drivers) are 300Ω and *15fF* respectively. The input gate capacitance (C_{rec}) of a receiver is 0.5 (pF). Two different supply voltages are selected

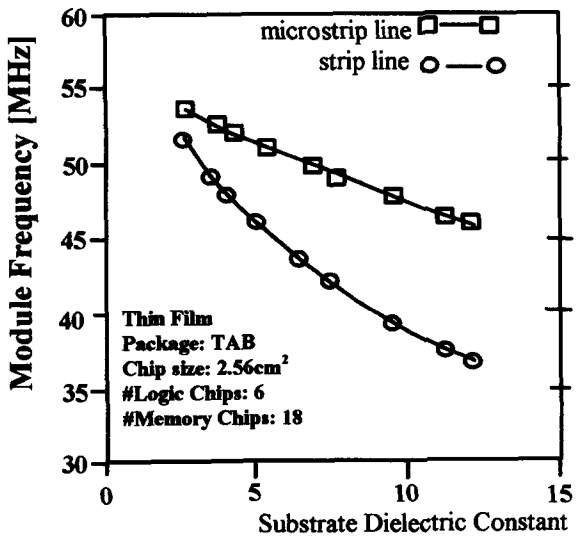


Figure 6a. Module frequency versus Various Dielectrics

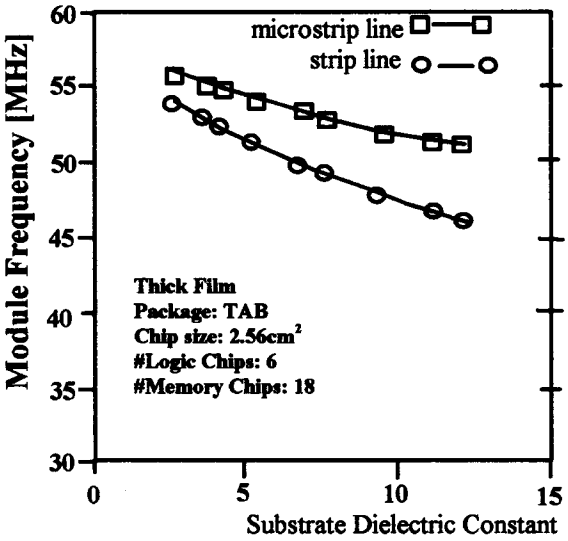


Figure 6b. Module Frequency versus Various Dielectrics.

- for this analysis: 1) V_{DD} = 5.0V and 2) V_{DD} = 3.3V.
- *Chip technology*: The maximum number of equivalent chips N_c integrated in an MCM is limited to 20 in this work. The average chip size ratio (logic chip over memory chip) is selected [17] to be 6. It is assumed that the clock frequency of a single chip (f_c) is 60 MHz. The worst case fanout f_o considered in this analysis is equal to (N_c - 1). Three different chip's footprint sizes are studied (with the corresponding number of I/O's per chip indicated in the parenthesis): 2.56cm^2 (180 I/Os), 4.0cm^2 (400 I/Os), 5.76cm^2 (600 I/Os).
- Bonding technology: TAB (Tape Automated Bonding) package technology with selected equivalent capacitance value C_{pad} = 1.5 (*pF*) is applied throughout all the cases in this section.
- *Parameters for SSN calculation*: In this work, it is assumed that each CMOS chip has 180 I/O chip-package connections, and 10 % of these total connections (N_p) are V_{SS} connections. To represent the present workstation application CMOS MCMs, a 32-bit data and address bus, and the following chip-package inductance values were used; 1) $L_{c\text{-}p}$ =1.0 (nH), 2) L_{plane}= 0.1 (nH), 3) L_{via}=1.5 (nH), and 4) L_{pin}=1.5 (nH). The maximum output current drive strength of 16.0 mA (D.C. sink when V_{ol}=0.4V) was used for the output drivers. One micron (L_{eff}=1μm) CMOS technology was used in all of chips in these MCMs. Two different supply voltage was selected [11]; 1) V_{DD}=5.0V, V_t=±0.9V,

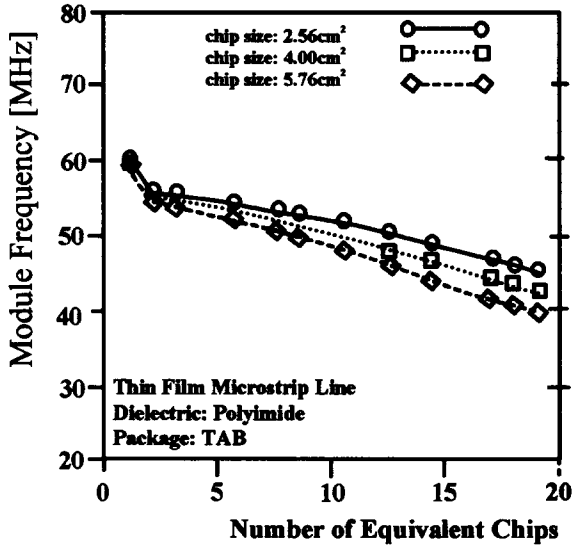


Figure 7a. Module Frequency versus Number of Chips for Microstrip line

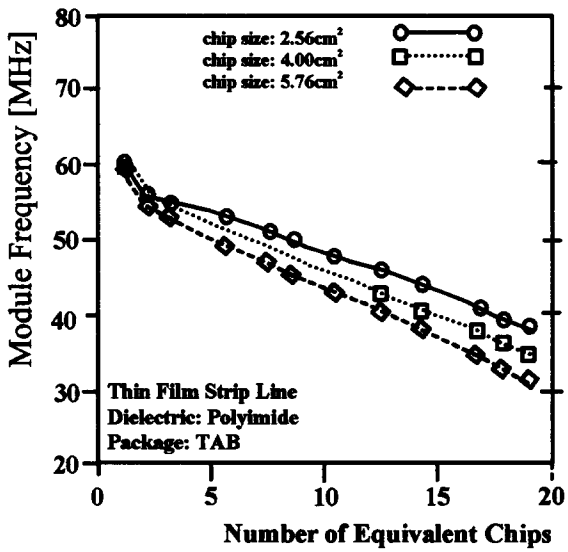


Figure 7b. Module Frequency versus Number of Chips for Strip line

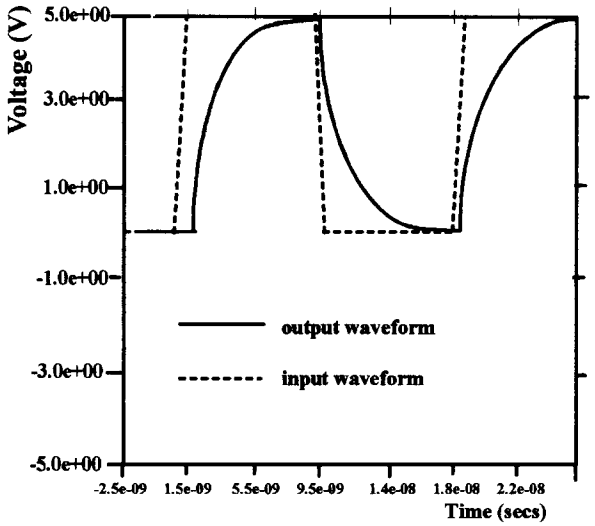


Figure 8. The transient response of the equivalent circuit.

and T = 1.0ns, and 2) V_{DD} = 3.3V, V_t = ±0.6V, and T = 0.7ns for SSN calculations.

The dependencies between module frequency and substrate dielectric constant are shown in Fig.6(a) and Fig.6(b) for thin film and thick film technologies respectively. For a given chip set (6 logic chips and 18 memory chips) and interconnect/package technology, the degrading trend of module frequency M_f (as the dielectric constant increases) can be seen from the plot. For the case of thin film microstrip in this example, use of Polyimide (ε_r = 3.5) over Alumina (ε_r = 9.5) as a substrate can improve module frequency by approximately 10%. The trade-offs between using microstrip line and strip line can also be studied from analyzing the curves for a given substrate dielectric material.

The following case study illustrates the concept of the use of both global and local analyses introduced in Figure 1. Usually for an MCM system design, functionality of the module can be implemented by either integrating fewer large sized chips (for example, VLSI chips) or more medium sized chips (LSI chips) in a module. Fig.7(a) and Fig.7(b) can be used to analyze these trade-offs. Because of the increase in off-chip interconnect length (when integrate more chips and the individual chip size becomes larger) and the number of fanouts, module frequency degrades (from the maximum frequency (f_c) of an individual chip) as the chip integration level increases. Assume point A in Fig.7(a) is a satisfactory (pre-selected) MCM configuration (module frequency M_f=52.5MHz,

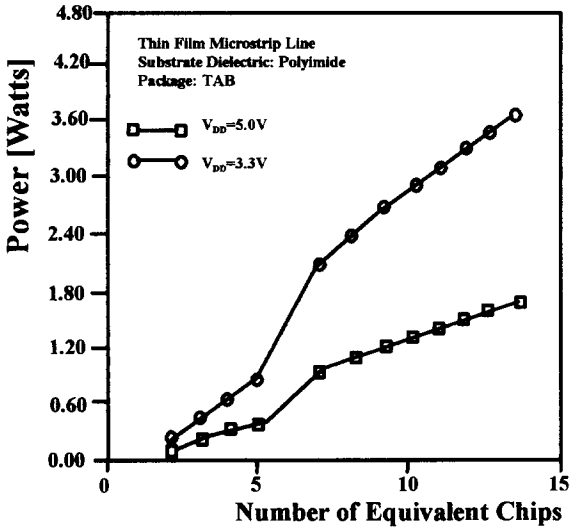


Figure 9. Power Dissipation versus Number of Chips.

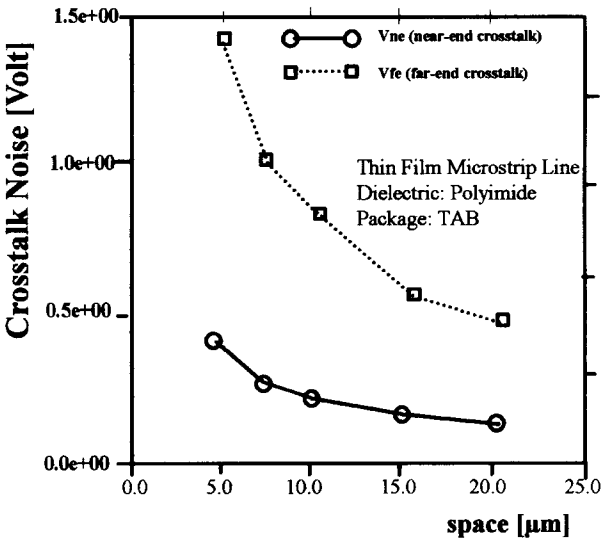


Figure 10a. Crosstalk Noise versus Conductor Space.

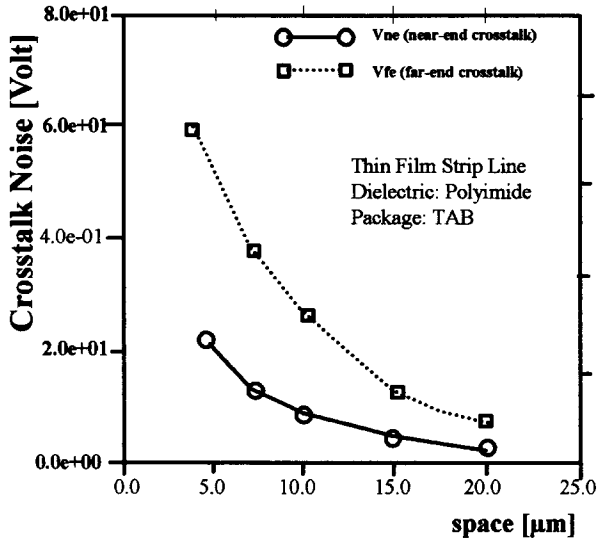


Figure 10b. Crosstalk Noise versus Conductor space.

L_{int}= 9.6cm, footprint size =2.56cm^2, N_c=9) after global analysis. It is then localized for further detailed analysis. A detailed transmission line circuit simulator called UANTL [18] is used to study the waveform of point A. Fig 8 shows the transient response of interested point A (represented by its equivalent circuit) when a 5V, 60 MHz input waveform with a rise time (T_r) and fall time (T_f) both equal to 0.5ns is applied.

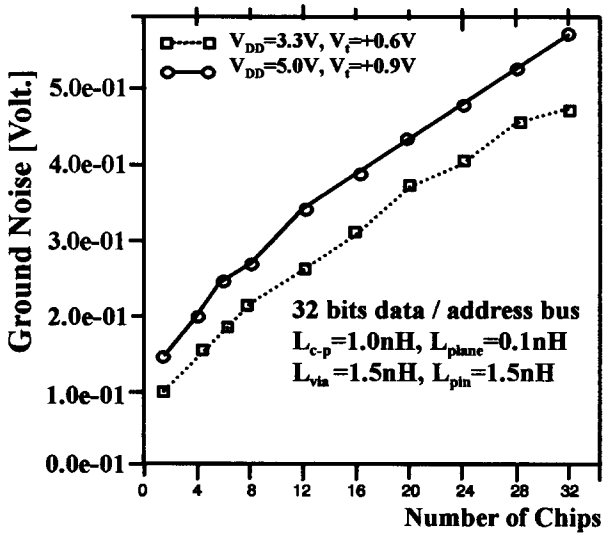


Figure 11. Ground Noise versus Number of Chips

The input waveform is generated at probe point 1 and the output waveform is observed at probe point 4 specified in Fig 2. The module frequency calculated by using detailed simulation tool is 52.9 MHz (measured the 70% delay from Fig 8), which is close to the value predicted by our simple model.

Power dissipation is also an important performance limiting factor for MCM applications. As the integration level of an MCM increases, total power dissipation of the module increases. Fig.9 shows the increasing trend of the power dissipation as more chips are integrated in an MCM. The percentage of the interconnects that switches (F_D) is assumed to be 50% for both cases (V_{DD} = 5.0V, and V_{DD} =3.3V). The slight power jumps in the curves are due to the increase of number of driver's cascaded stages, which is necessary because larger fanouts need to be driven. This can also be explained by equation (5). Even though power consumption is less for the case of reduced supply voltage (3.3V), noise problem might become critical because of the increased noise to signal ratio.

In order to increase the integration level in an MCM, interconnect density is usually increased. However, trade-off must be made so that the associated increase of the coupled noise between coupled transmission lines won't cause any false switching in a circuitry. Again, point A in Fig.7(a) is taken for further investigation of the effect of coupled noise. Near-end (V_{ne}) and far-end (V_{fe}) crosstalk values are calculated using transmission line simulator UANTL for five different conductor spaces (s=0.5w, s=0.8w, s=w, s=1.5w and s=2.0w).

The coupled transmission line system in Fig.2 with interconnect length L_{int}= 9.6cm is used as the equivalent circuit for the study of crosstalk. The far-end and near-end crosstalk on the quiet line for both the cases of thin film microstrip line and strip line are shown in Fig.10(a) and Fig.10(b) respectively. Note that, if the noise to signal ratio exceeds the maximum allowable value, unwanted false switching of the receiver might happen in the circuit.

Fig.11 shows the dependency between SSN and MCM

integration level. It is clear that SSN increases with the increase in integration level. Note that, for a given output driver current strength (16 mA in this work), when output drivers switch simultaneously, SSN is larger for reduced supply voltage (3.3 V) MCMs than the 5.0 V supplied ones. For a given MCM design, it is essential to estimate and reduce SSN within the maximum allowable SSN to avoid the false switchings. This is even more important for MCMs with scaled CMOS devices and/or reduced supply voltage.

IV. RELATED WORK

Not many tools exist in the area of early design for multichip modules. None consider noise as a performance-limiting factor and none are integrated with detailed simulation environment for further analysis which is essential for practical MCM early designs.

Developed at Stanford University, SUSPENS [19] is basically an analytical model that takes some material, device, circuit, logic, package, and architecture parameters as inputs and using them calculates the clock frequency, module size and power dissipation of the system, as well as several other detailed parameters. The results of this work have been compared with existing microprocessors, and used to predict the performance of future microprocessors. Some of the equations for calculating the module frequency have been modified and included in our simulation environment.

AUDiT [20] is a package system simulation software used to study multi--chip module trade-offs. Modules in AUDiT are described with a set of structural, electrical and materials related model parameters. Simulated annealing technique is applied to determine the structure and technologies required for a optimal (minimum cycle time) system. Three packaging hierarchies (single chip, module, and board) based on CMOS technology have been used as demonstration systems. Logic and memory subsystems were treated separately in this work.

SPEC [21] is designed to compute geometric, electrical, thermal, and manufacturing(cost) performance metrics specifically for multichip systems. The estimations used in SPEC "are based on those previously developed in recent literature " [21]. For electrical performance, the system did not include noise as a performance-limiting factor. The system also lacks more detailed simulation tools to analyze the effects of signal degradation and reflection which can not be estimated or predicted from first order closed-form equations.

V. CONCLUSIONS

A knowledge-based simulation environment has been developed for the early design of MCMs. The feasibility of the proposed approach has been demonstrated by evaluating the electrical system performance metrics of CMOS-based MCMs for workstation applications. This tool can be useful for the MCM system designers especially when rapid design evaluation is essential. Although only electrical performance metrics of MCMs are treated in this work, similar approach can be applied to other multichip assembled applications such as COB (chip on board). Future work will include performance schedules of other aspects for MCM system design such as thermal, mechanical and reliability.

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